COE 202: Digital Logic Design
Combinational Circuits
Part 4

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Objectives

- Magnitude comparator
  - Design of 4-bit magnitude comparator
- Design Examples using MSI components
  - Adding Three 4-bit numbers
  - Building 4-to-16 Decoders with 2-to-4 Decoders
  - Getting the larger of 2 numbers (Maximum)
  - Excess-3 Code Converter

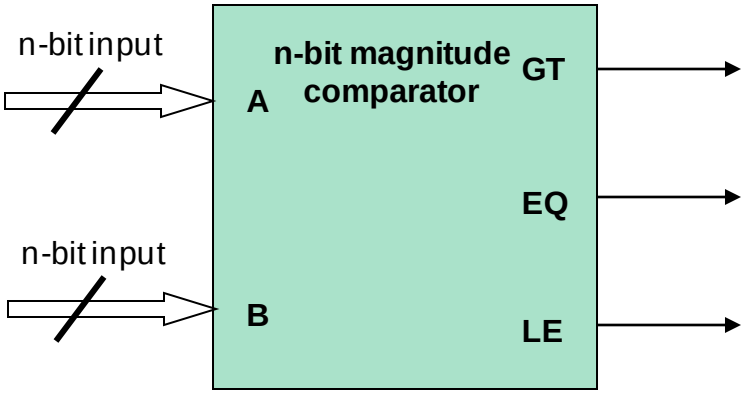
Magnitude Comparator

Definition: A magnitude comparator is a combinational circuit that compares two numbers A & B to determine whether:

A > B, or

A = B, or

A < B



Inputs

First n-bit number A

Second n-bit number B

Outputs

3 output signals (GT, EQ, LT), where:

GT = 1 IFF A > B

EQ = 1 IFF A = B

LT = 1 IFF A < B

Note: Exactly One of these 3 outputs equals 1, while the other 2 outputs are 0`s

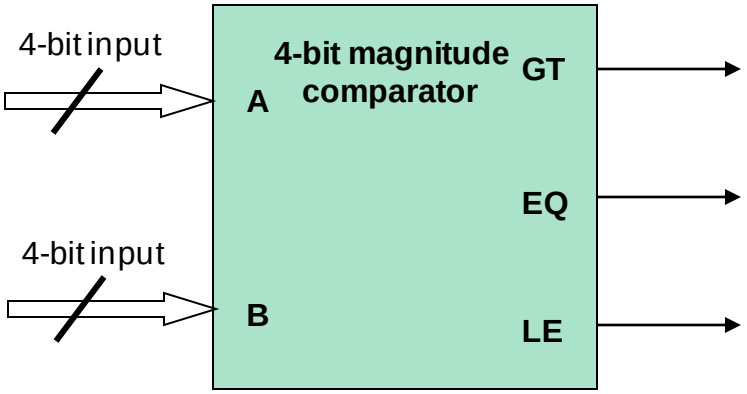
Example 1: Magnitude Comparator (4-bit)

Problem: Design a magnitude comparator that compares 2 4-bit numbers A and B and determines whether:

A > B, or

A = B, or

A < B



Example 1: Magnitude Comparator (4-bit)

Solution:

Inputs: 8-bits (A ⇒ 4-bits , B ⇒ 4-bits)

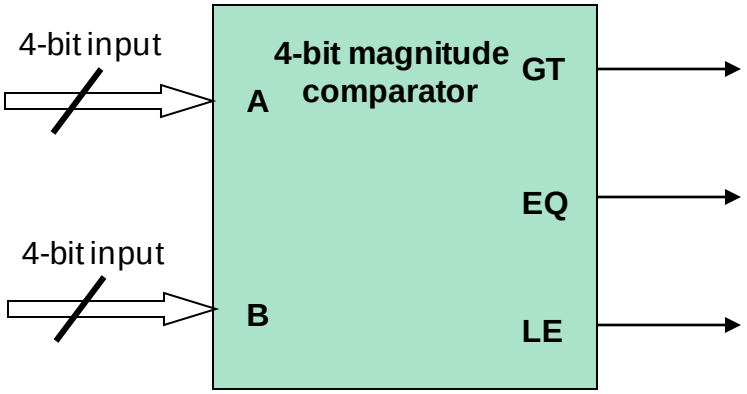
A and B are two 4-bit numbers

Let $A = A_3A_2A_1A_0$, and

Let $B = B_3B_2B_1B_0$

Inputs have 2^8 (256) possible combinations (size of truth table and K-map?)

Not easy to design using conventional techniques



The circuit possesses certain amount of regularity
⇒ *can be designed algorithmically*.

Example 1: Magnitude Comparator (4-bit)

Designing EQ:

Define $X_i = A_i$ **xnor** $B_i = A_i B_i + A_i' B_i'$

➔ $X_i = 1$ IFF $A_i = B_i$ $\forall$ i =0, 1, 2 and 3

➔ $X_i = 0$ IFF $A_i \neq B_i$

Therefore the condition for A = B or EQ=1 IFF

$A_3 = B_3 \rightarrow (X_3 = 1)$, and

$A_2 = B_2 \rightarrow (X_2 = 1)$, and

$A_1 = B_1 \rightarrow (X_1 = 1)$, and

$A_0 = B_0 \rightarrow (X_0 = 1)$.

Thus, EQ=1 IFF $X_3 X_2 X_1 X_0 = 1$. In other words,

$$EQ = X_3 X_2 X_1 X_0$$

Example 1: Magnitude Comparator (4-bit)

Designing GT and LT:

GT = 1 if A > B:

- If $A_3 > B_3 \rightarrow A_3 = 1$ and $B_3 = 0$
- If $A_3 = B_3$ and $A_2 > B_2$
- If $A_3 = B_3$ and $A_2 = B_2$ and $A_1 > A_1$
- If $A_3 = B_3$ and $A_2 = B_2$ and $A_1 = B_1$ and $A_0 > B_0$

Therefore,

$GT = A_3B_3' + X_3 A_2 B_2' + X_3 X_2 A_1 B_1' + X_3 X_2 X_1A_0 B_0'$

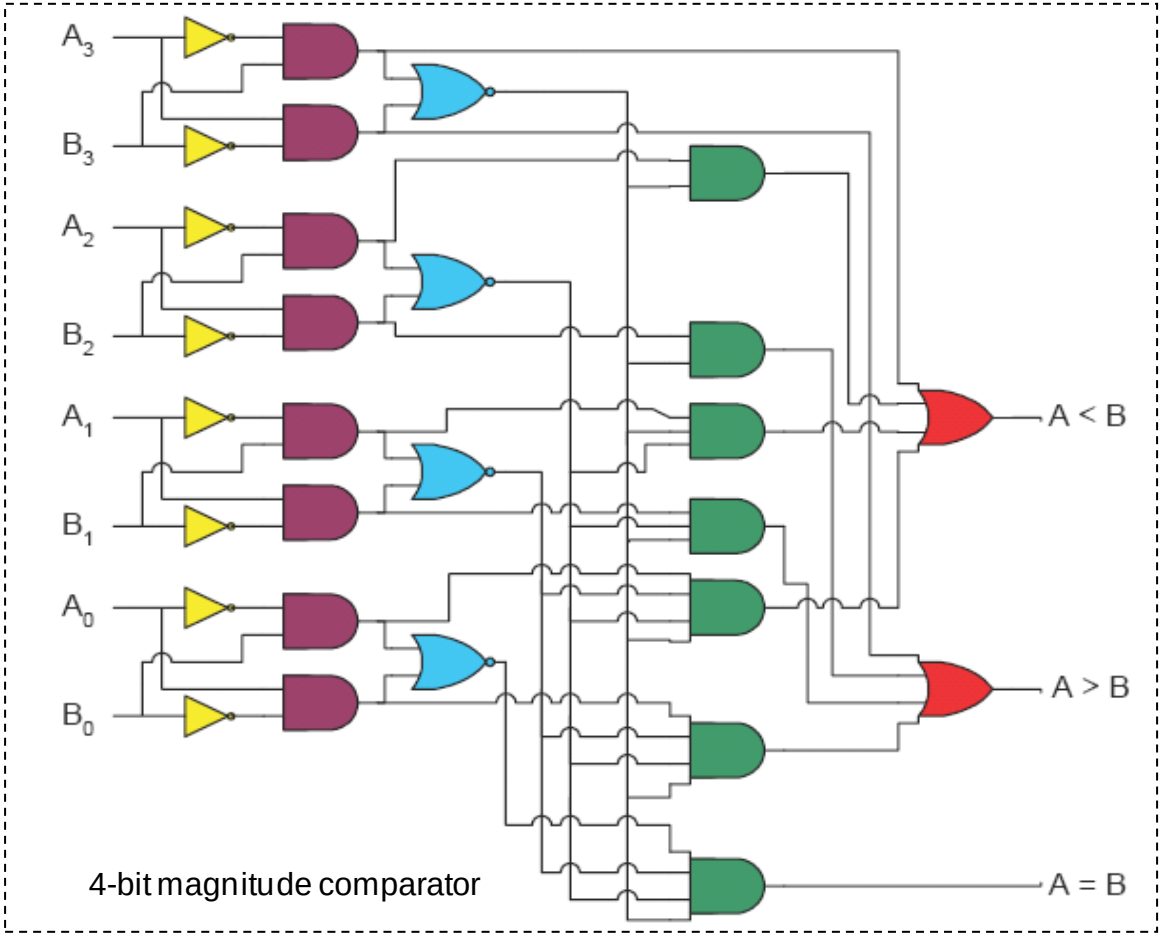
Similarly, $LT = A_3'B_3 + X_3 A_2'B_2 + X_3 X_2 A_1'B_1 + X_3 X_2 X_1A_0' B_0$

Example 1: Magnitude Comparator (4-bit)

$EQ = X_3\ X_2\ X_1\ X_0$

$GT = A_3B_3'$
$\quad + X_3A_2B_2'$
$\quad + X_3X_2A_1B_1'$
$\quad + X_3X_2X_1A_0B_0'$

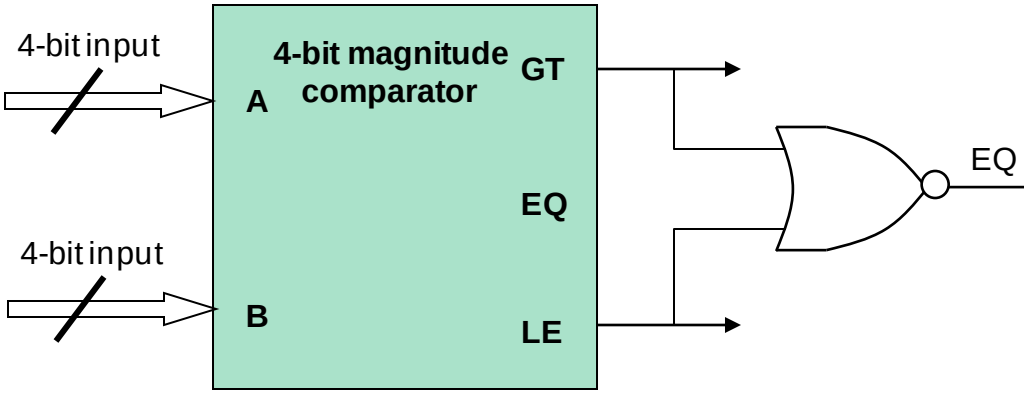
$LT = B_3A_3'$
$\quad + X_3B_2A_2'$
$\quad + X_3X_2B_1A_1'$
$\quad + X_3X_2X_1B_0A_0'$



4-bit magnitude comparator

Example 1: Magnitude Comparator (4-bit)

- Do you need all three outputs?
- Two outputs can tell about the third one
  - Example: when A is NOT GREATER THAN B, and A is NOT LESS THAN B THEN A is EQUAL TO B
- Therefore, we can save some logic gates:



Example 2: Adding three 4-bit numbers

Problem: Add three 4-bit numbers using standard MSI combinational components

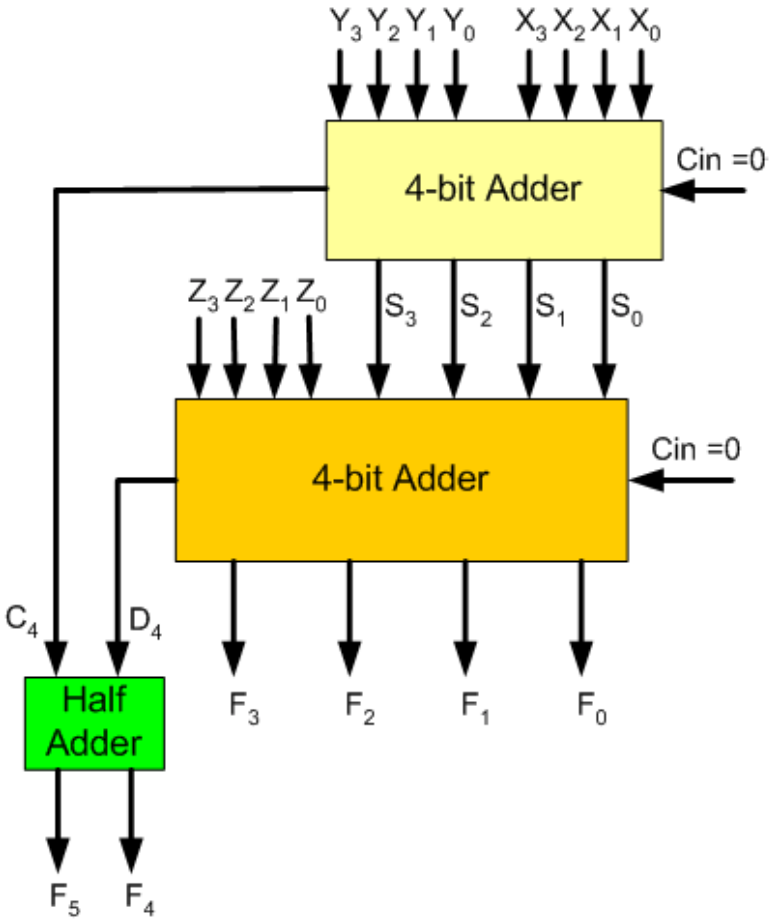
Solution:

Let the numbers be $X_3X_2X_1X_0$, $Y_3Y_2Y_1Y_0$, $Z_3Z_2Z_1Z_0$,

$$
\begin{array}{rl}
 & X_3X_2X_1X_0 \\
+ & Y_3Y_2Y_1Y_0 \\
\hline
C_4 & S_3S_2S_1S_0
\end{array}
\qquad\qquad
\begin{array}{rl}
 & S_3S_2S_1S_0 \\
+ & Z_3Z_2Z_1Z_0 \\
\hline
D_4 & F_3F_2F_1F_0
\end{array}
$$

Note: C_4 and D_4 is generated in position 4. They must be added to generate the most significant bits of the result

Example 2: Adding three 4-bit numbers



Example 3: 4-to-16 Decoder

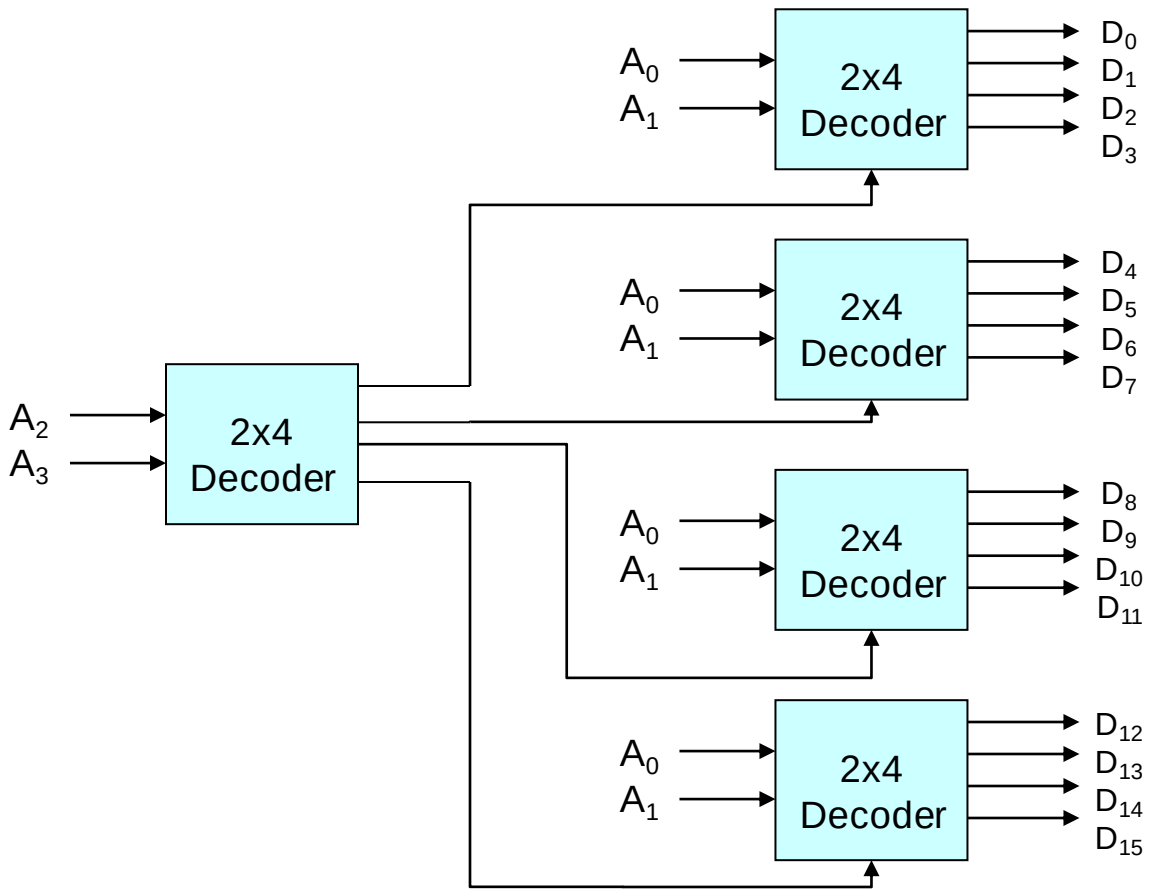
Problem: Design a 4x16 Decoder using 2x4 Decoders

Solution:

- Each group combination holds a unique value for A_3A_2
- One Decoder can be therefore used with inputs: A_3A_2
- Four more decoders are needed for representing each individual color combination

	A_3	A_2	A_1	A_0	Output
$A_3A_2 = 00$	0	0	0	0	D_0
	0	0	0	1	D_1
	0	0	1	0	D_2
	0	0	1	1	D_3
$A_3A_2 = 01$	0	1	0	0	D_4
	0	1	0	1	D_5
	0	1	1	0	D_6
	0	1	1	1	D_7
$A_3A_2 = 10$	1	0	0	0	D_8
	1	0	0	1	D_9
	1	0	1	0	D_{10}
	1	0	1	1	D_{11}
$A_3A_2 = 11$	1	1	0	0	D_{12}
	1	1	0	1	D_{13}
	1	1	1	0	D_{14}
	1	1	1	1	D_{15}

Example 3: 4-to-16 Decoder

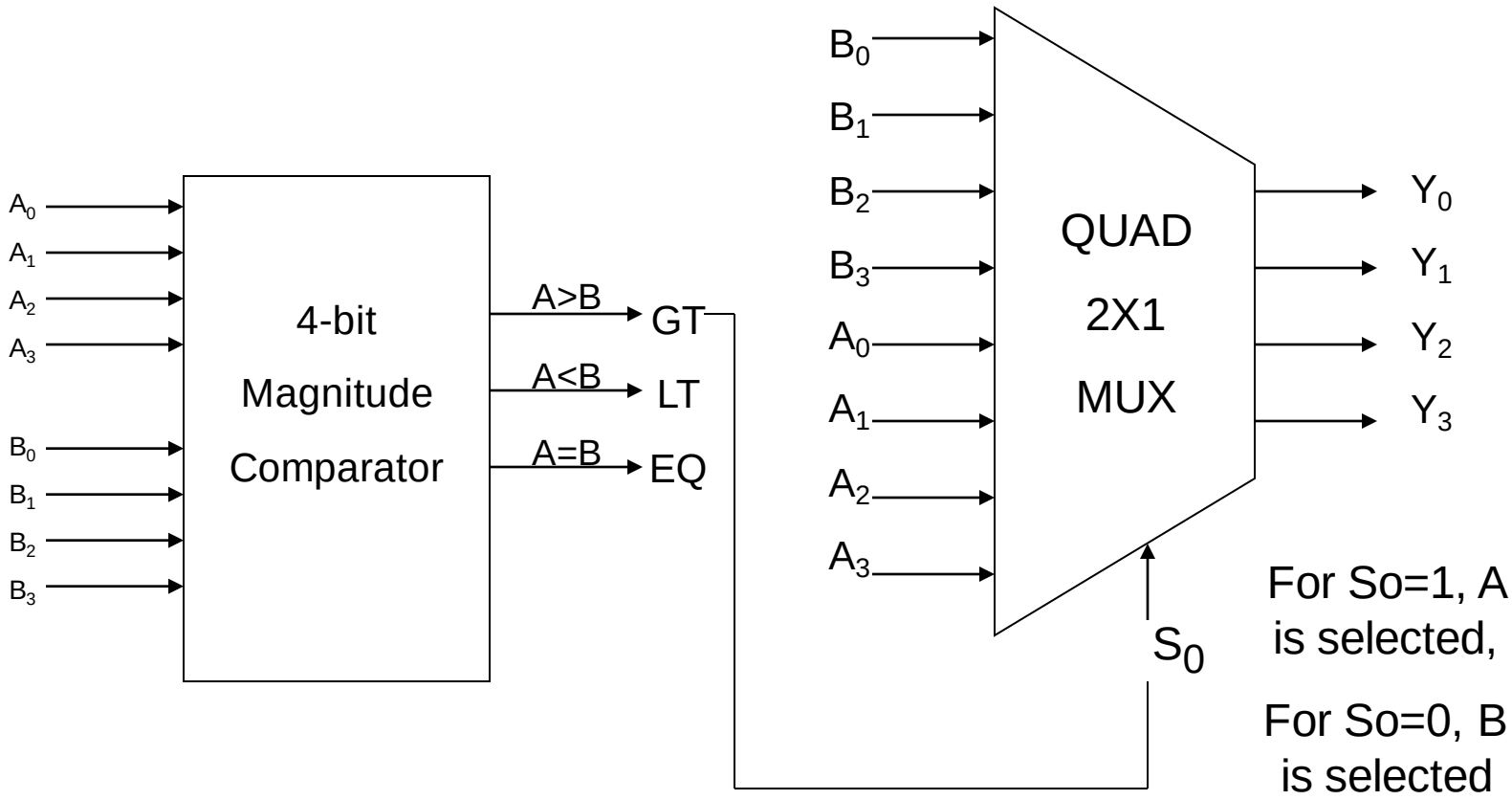


Example 4: The larger of 2 numbers

Problem: Given two 4-bit unsigned numbers, design a circuit such that the output is the larger of the two numbers

Solution: We will use a magnitude comparator and a Quad 2x1 MUX. How?

Example 4: The larger of 2 numbers



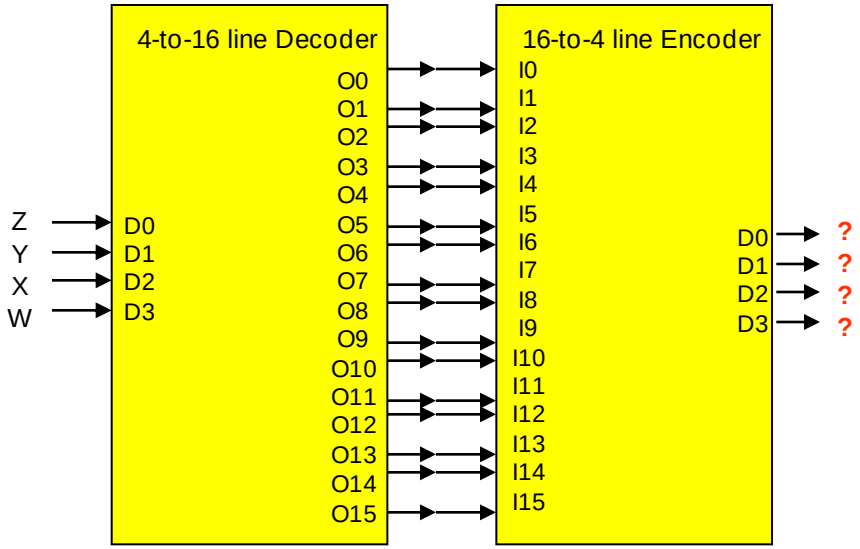
Example 5: Excess-3 Code Converter

Problem: Design an excess-3 code converter that takes as input a BCD number, and generates an excess-3 output.

Solution: Use decoders and encoders

W	X	Y	Z	A	B	C	D
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

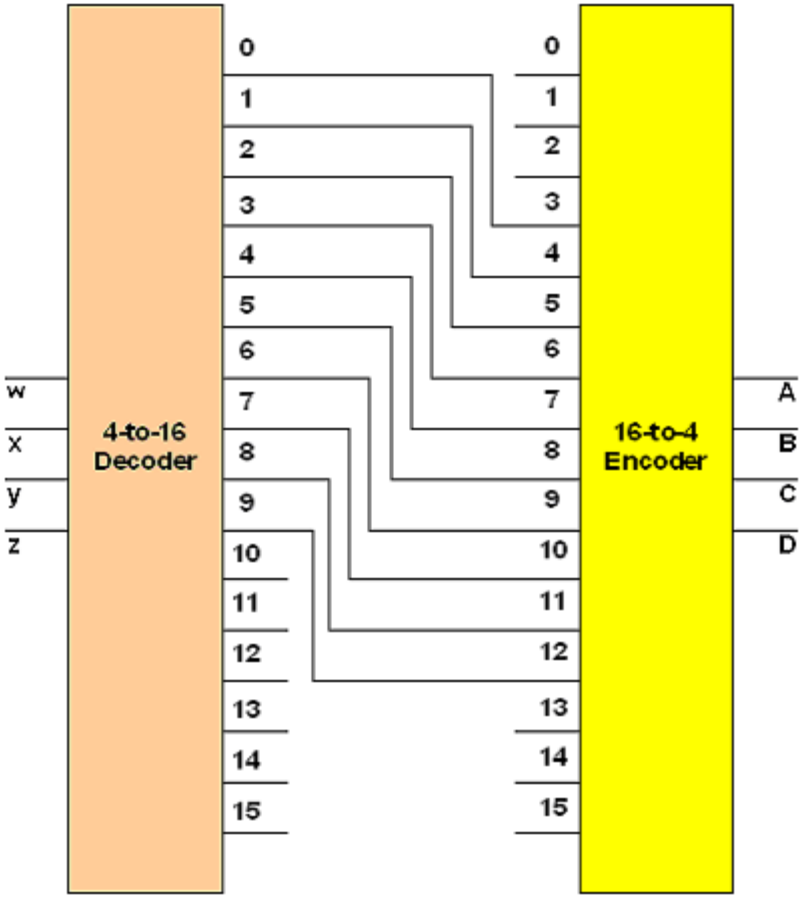
Example 5: Excess-3 Code Converter



What will be the output?

Example 5: Excess-3 Code Converter

- A decoder can be used with the inputs being W,X,Y,Z
  - It will be a 4x16 decoder, with only a single output bit equal to 1 for any input combination
- An encoder (16x4) will take as input the 16 bit output from the decoder, and will generate the appropriate output in excess-3 format
- For this to function correctly, the output from the decoder must be displaced 3 places while being connected to the encoder input
- It may be noted that outputs 10,11,12,13,14,15 of the decoder are not used – since we are dealing with BCD



Summary

- Design = Different possibilities
- Better designer = more practice
- More design examples in the textbook