Objectives
- Design and implementation of a combinational circuit
- Learning about the onboard clock and clock division
- Using buses and bus taps in ISE

Description
The rear lights of a car are to be controlled by a digital logic circuit. There is a single lamp in each of the rear lights.

The inputs to the controller are:
- LT: left turn switch – causes blinking of the lift side lamp
- RT: right turn switch – causes blinking of the right side lamp
- EM: Emergency flasher switch – causes blinking of both lamps
- BR: Brake applied switch – causes both lamps to be on
- BL: blinking signal of 1Hz frequency

The outputs of the controller are:
- LR: power control for left rear lamp
- RR: power control for right rear lamp

Clock Divider
Our board has a built-in clock of 50Mhz (pin T9). It is possible to generate slower clocks using a binary counter as shown in the figure.

\[
\frac{C}{2^n}
\]

In general, a slower clock can be derived from the \( n \)th bit of the counter. The frequency is given by

\[
F = \frac{C}{2^n}
\]
Lab Activities

Part 1. Variable Clock Generator (20 points):

1. Build a new schematic symbol which can generate the frequencies 0.5Hz, 1Hz, 2Hz and 4Hz. The symbol has an input clock and four output clocks. Use two cascading counters (CB16CE) to build this symbol.
2. Using a 4x1 MUX (M4_1E) and the above symbol, implement a circuit to select one of the frequencies and display it on an LED.

Part 2. Light Controller (30 points):

1. Obtain the truth table of LR(LT, EM, BR, BL) and RR(RT, EM, BR, BL). Assume the following
   1. BR overrides EM
   2. LT and RT override BR
2. Implement LR and RR using two 4-to-16 decoders and OR gates.

Lab Report
Use the provided template to write your report.

Discussion Questions

- The explained clock divider is limited to powers of two for clock division. How can you extend it to divide a frequency by any integer value?
- Show how the controller can be implemented with MUXs. Which approach is better and why?