COE 203: Digital Logic Laboratory
Term 092 (Spring 2010)

Syllabus

Section: 54  Time: T 11:00-14:00  Place: 22-340A

Instructor: Dr. Ahmad Almulhem  Office: 22-324
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Office Hours: TBA

Course Description:
Review of Digital Logic Design: Design of Combinational Circuits, and Design of Sequential Circuits. Logic implementation using discrete logic components (TTL, CMOS), and programmable logic devices. Introduction to Field Programmable Logic Arrays (FPGAs). The basic design flow: design capture (schematic capture, HDL design entry, design verification and test, implementation (including some of its practical aspects), and debugging. Design of data path and control unit.

Course Prerequisite: COE 202


Learning Outcomes:
1. Build combinational and sequential circuits
2. Learn to use design tools
3. Introduction to Hardware Description Languages
4. Team work
5. Communicate effectively

Grading:

- Lab Work: 75% (5 Experiments)
  - Each Experiment (40% Implementation, 10% Simulation, 25% Report)

- Project: 20%

- Attendance: 5%

Tentative Schedule:

- Digital logic design review  W2
- Introduction to FPGA Design Tools  W3
- Design with FPGA  W4 - W10
  - Combinational and Sequential
  - Schematic and HDL
- Project  W11 - W14

Important Remarks:

- Lab work will be carried in teams.
- Attendance will be checked each lab. 20% absences (3 labs) will result in a DN grade.
- Submissions must be your own work. Cheating is not tolerated and will result in an F grade.
- All KFUPM regulations and standards are enforced.