1.0

Himawari
Design Proposal

Prepared by:

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Revision History

Date	Rev	Details
10-29-2014	0.7	First Draft
11-3-2014	1.0	Initial Release

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Objectives

The objective of this project is to design an FPGA based controller for a dual axis sun tracking system that can increase the utilization of solar panels.

Introduction

Rawabi United Safety Services produces gas detection systems, each gas detection system consists of several gas detection stations. Those stations are usually operating in the middle of the desert, where there is no power lines. A station operating at the middle of the desert is powered by a rechargeable battery, which is charged by a large solar panel. The use of large solar panels increases the cost of each station significantly, and make it hard to move stations from one place to another. Furthermore, during cloudy days, if some of the cells of a solar panel are shaded this will significantly reduce the electricity being generated, or even eliminate it. This is due to the fact that cells of a solar panel are connected as a string (in series), a solar panel could contain one string or more of cells, but small solar panels are usually composed of one string. This issue affects the reliability of the systems noticeably during cloudy days.

This project will investigate the application of sun tracking to increase the utilization of solar panels, increase the reliability of the gas detection systems and decrease their costs,

Design Requirements

- Dual axis sun tracking.
- Based on FPGA.
- Reduce the number of ICs as much as possible.
- Keep track of the orientation of the solar panel.
- Tracking the sun without human intervention.
- An option for locking the position of the solar panel.
- Auto calibration.
- Solar panel weight (5.7 kg).
- Can withstand wind and compensate.
- SPI Interface to allow external system to:
    - Control the position of the solar panel.
    - Get sensors’ readings.
    - Get the orientation of the solar panel.
- Movement of solar panel using servo motors.

Preliminary Specifications

Parameter	Specifications
FPGA Chip	Altera MAX10
Tracker Type	Active dual-axis sun tracker
Tracking Method	Based on light sensors and time.
Motors	Two servo motors with analog feedback
Light Sensors Type	To be decided.
Communication Interface	SPI
Operating Temperature	-40°C ~ 85°C

Design Approach

This design will track the sun by four light sensors mounted on the solar panel and keeping track of the time of the day. Two servo motors will be used to move the solar panel in two axes. Servo motors with analog feedback signal will be used to provide accurate orientation of the solar panel, auto calibration for the orientation of the solar panel and to compensate the effect of the wind or any other mechanical issues. The servo motors will be driven using a module to be designed and implemented on the FPGA chip, due to the fact that FPGAs are perfect for motor control and the need to reduce chip count.

Preliminary Design Description

Design Architecture

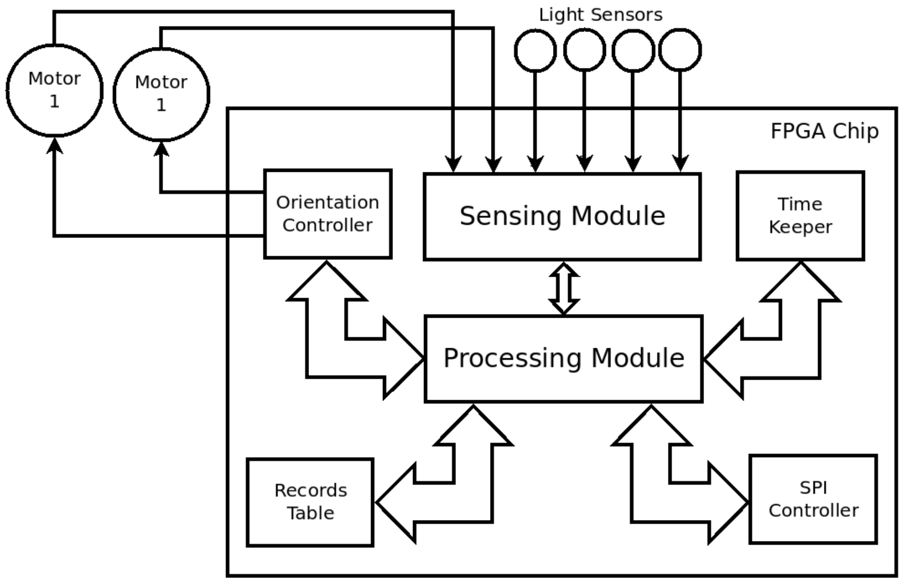

Figure 1: Design architecture of the sun tracking controller

Figure 1 shows the general architecture of the sun tracking controller. As depicted in figure 1, the design of the sun tracking controller can be divide into 6 main modules all to be implemented on one FPGA chip:

1. Sensing Module
   Provides six analog channels to measure the output of four light sensors and two feedback motor signals.
2. Orientation Controller Module
   Controls the movement of the motors and keeps track of the orientation of the solar panel.
3. Time Keeper Module
   Keeps track of the time of the day.
4. Knowledge Base Module
   Will be used by the processing module to store the optimum position of the solar panel for several periods of the day.
5. Processing Module
   - Will process the readings from the light sensors to determine whether it is day time or night time and will send the result to the time keeper.
   - Will process the feedback signals from the motors.
   - Will process the information provided by the time keeper.

- Will record tracking data in the knowledge base to build its knowledge, and will process this collected data when taking decisions.
- Will take the decisions to move the solar panel based on the results of the processed data.
- Will communicate with external systems through the SPI interface to provide live readings of registers and manual control of position of the solar panel by the external system.

6. SPI Interface Module
   Will be responsible for delivering messages between the processing module and an external system through an SPI bus.

Component Design

Sensing Module

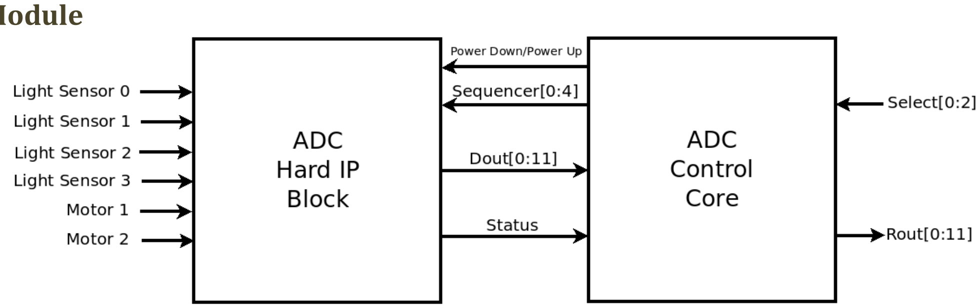

Figure 2: Organization of the sensing module

The sensing module will be used to interface the light sensors and read the feedback signals from the motors. This module is composed of two main components, the ADC hard IP block, and an ADC control core. The ADC hard IP block is a hard part of the MAX 10 FPGA chip that contains the ADC circuit and will get the readings from the analog devices. The ADC control core is a soft block that will be designed and implemented, it will control the operation of the ADC and will act as an abstraction layer between the processing module and the ADC.

Orientation Controller Module

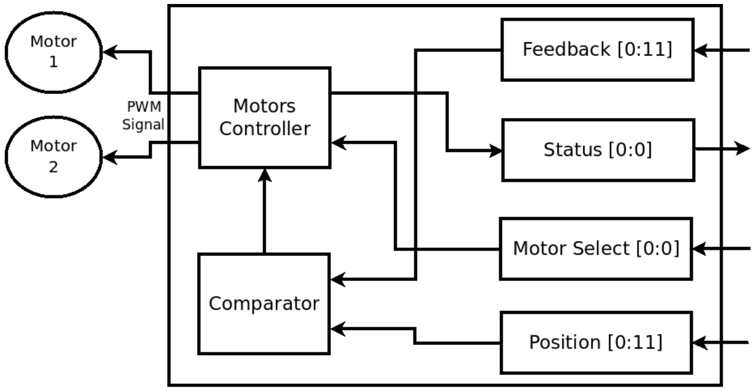

Figure 3: Organization of the orientation controller

The orientation controller is composed of the following main sub components:

a. Motors controller: will generate a pulse width modulation (PWD) signal to drive the selected motor, and will output the Status signal to indicate whether it is busy driving a motor or not.
b. Comparator: will compare the position feedback signal from the selected motor with the required position by the processing module, and based on that comparison will generate a signal to the motors controller to specify the direction of the movement.

Time Keeper Module

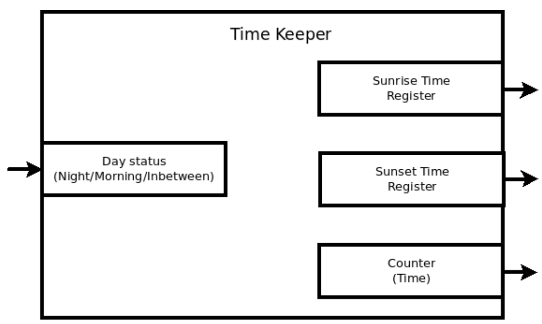

Figure 4: Time Keeper's inputs and outputs

The time keeper will keep track of the time in a fuzzy way, and will provide three registers to be used by the processing module, as figure 4 shows: Sunrise Time Register, Sunset Time Register, and Counter or Time Register. The value stored in the Sunrise Time Register represents the sunrise time of the current day and the expected sunrise time for the following day, with respect to the clock of the time keeper. In the same manner, the value stored in the Sunset Time Register represents the sunset time of the current day and the expected sunset time for the following day, with respect to the clock of the time keeper. On the other hand, the counter register contains the time of day with respect to the clock of the time keeper, it stores the hours and minutes. The time keeper uses the status of day (night, morning, or in-between) reported by the processing module in the Day Status register, to apply the algorithm that keeps track of the time and determines the sunrise time and the sunset time.

The flowchart below describes the algorithm that will applied by the time keeper to keep track of time. As the flowchart depicts, the time keeper will calibrate itself everyday based on the sunrise of each day.

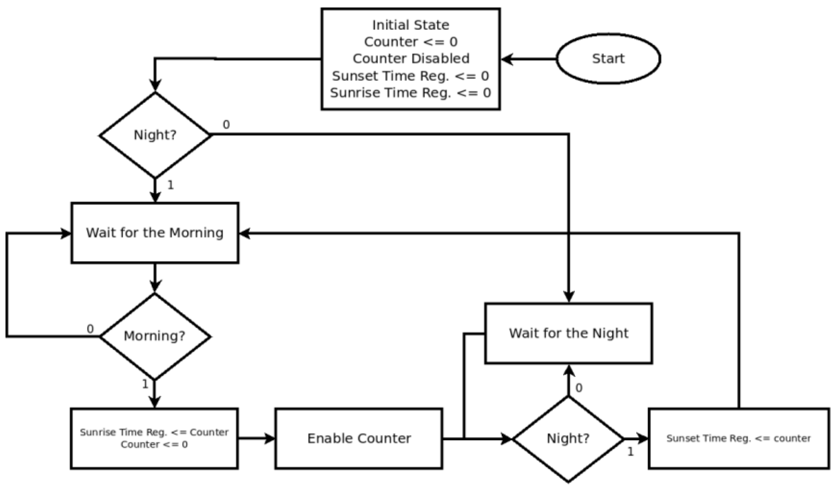

Figure 5: Time keeper's algorithm

Records Table Module

Hour	Minute	Position X	Position Y
1	00	106	154
1	15	110	160
1	30	115	160
….	….	….	…

Figure 6: Records table organization

This module will store a table containing the time with respect to the sun tracking controller clock, and the corresponding optimum position for the solar panel. The processing module will access a record by passing an address to the record table module through the address register, and reading/writing the content through the data bus.

Processing Module

Design not finished yet.

SPI Controller Module

The SPI controller will apply the following algorithm to handle the communications between the processing module and the external system through the SPI bus:

- If request is received
- The SPI controller processes the request
- If valid request,
    - If write request
        - The SPI controller sends a register address to the processing module.
        - The SPI controller puts the data on the data bus.
        - the SPI controller sends an interrupt signal with a write request to the processing module

A read request will be handled in a similar way.

Schedule

Task Name	Duration	Start	Finish	Resource Names	% Complete
Development of Himawari	**41 days**	**Sun 10/26/14**	**Fri 12/5/14**		**2%**
Development of the Controller	**30 days**	**Wed 10/29/14**	**Thu 11/27/14**		**6%**
Sensing Module	3 days	Wed 10/29/14	Fri 10/31/14	Murtadha	50%
Orientation Controller Module	3 days	Wed 11/5/14	Sat 11/8/14	Murtadha	0%
Time Keeper Module	3 days	Sun 11/9/14	Tue 11/11/14	Murtadha	0%
Sun Tracking Learning Algorithm Module	3 days	Wed 11/12/14	Fri 11/14/14	Murtadha	0%
SPI Interface	3 days	Sat 11/15/14	Mon 11/17/14	Murtadha	0%
Testing each module (primary debugging)	2 days	Tue 11/18/14	Wed 11/19/14	Murtadha	0%
Integrating Controller Modules	5 days	Thu 11/20/14	Mon 11/24/14	Murtadha	0%
Testing the Controller (Secondary Debugging)	3 days	Tue 11/25/14	Thu 11/27/14	Murtadha	0%
Controller Development Complete	0 days	Thu 11/27/14	Thu 11/27/14	Murtadha	0%
Solar Panel Movement System	**32 days**	**Sun 10/26/14**	**Wed 11/26/14**		**0%**
Solar Panel Movement System Requirements	2 days	Sun 10/26/14	Mon 10/27/14	Qusay	0%
Solar Panel Movement System Design Proposal	5 days	Tue 10/28/14	Sat 11/1/14	Qusay	0%
Designing the Solar Panel Movement System	9 days	Sun 11/2/14	Mon 11/10/14	Qusay	0%
Manufacturing of the Solar Panel Movement System	14 days	Tue 11/11/14	Mon 11/24/14	Qusay	0%
Installing the Solar Panel Movement System	2 days	Tue 11/25/14	Wed 11/26/14	Qusay,Rakan	0%
Solar Panel Movement System Installed	0 days	Wed 11/26/14	Wed 11/26/14		0%
Integrating the Controller and the System	3 days	Fri 11/28/14	Sun 11/30/14	Murtadha	0%
Final Debugging	5 days	Mon 12/1/14	Fri 12/5/14	Murtadha	0%
System Development Complete	0 days	Fri 12/5/14	Fri 12/5/14		0%
Testing	**10 days**	**Sat 12/6/14**	**Mon 12/15/14**		**0%**
Testing	5 days	Sat 12/6/14	Wed 12/10/14	Rakan[50%],Murtadha[50%]	0%
Performance Verification	5 days	Thu 12/11/14	Mon 12/15/14	Murtadha[50%],Dr. Aiman[50%]	0%
Project Complete	0 days	Mon 12/15/14	Mon 12/15/14		0%