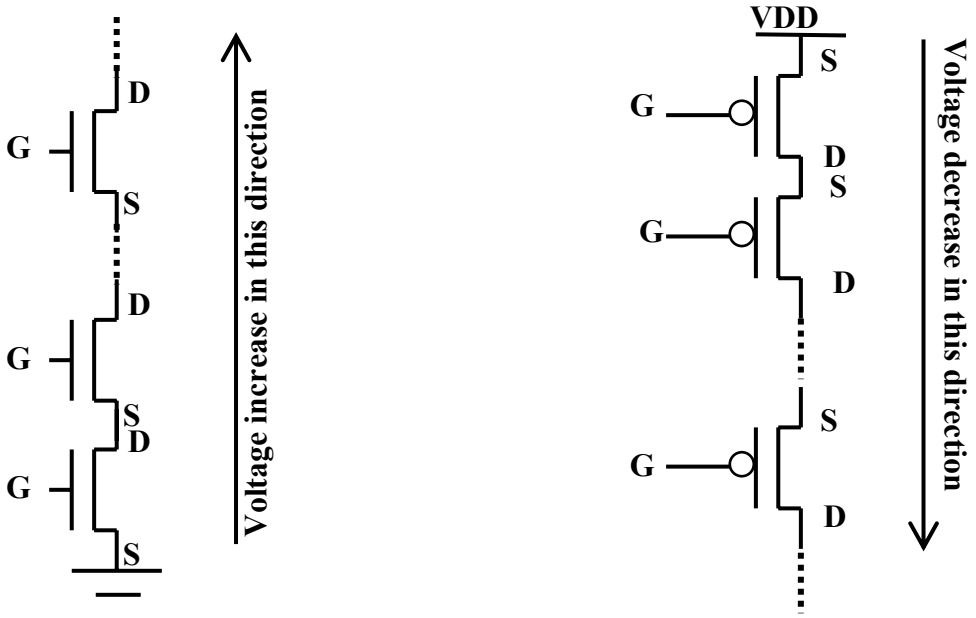
Hints for solving MOS Circuits

When solving MOS circuits follow the following procedure:

1. Identify the gate, source and drain terminals of all transistors. For NMOS, the drain is the node with higher voltage (i.e. closer to the supply voltage VDD). As for PMOS, the source is the node closer to the supply voltage.



2. Then examine VGS of each device: for NMOS If VGS < Vth --> then it is off for PMOS If VSG < |Vth| --> then it is off (note VSG not VGS), i.e. the source voltage of a PMOS has to be higher than the Gate voltage by -Vth ... So if Vth = -1V, then VSG has to be > 1 V for the PMOS to be on.
3. After establishing which device is On or Off, now try to establish which device is in saturation or linear regions (to use the appropriate current equation). Use KCL and substitute the current equations (which depends on the terminal voltages) and solve for voltages and currents.
4. If you can not establish weather a transistor is in linear or saturation, then assume saturation and solve. Then check your assumption, if it turns out to be wrong, re-solve with the transistor in linear. If you have more than one device (i.e. transistor) then you will have several possibilities to check (i.e. for 2 transistors that are ON, Sat. Sat., Sat. Lin., Lin. Lin. and Lin. Sat.

5. If a transistor has its gate and drain nodes tied together (i.e. VDS = VGS) than it will always be in saturation if it is ON.

Transistors that are always in saturation since their VDS = VGS