CSE670, Dr. Muhammad Elrabaa
Assignment #1, Due 27/3/2004

Review Problems:

Q1) Implement the following function using minimum # of 2-1 MUXs:

$$F = A + B \cdot C + D \cdot E$$

Q2) It is required to implement a 16-bit Adder using Full Adders that can operate at 800 MOPs (Mega operations per seconds). Assume that the FA's worst case delay is 200 pS, the flip-flops Clk → Q delay is 150 Ps, its setup time is 125 Ps, its hold time are 100 Ps, and the clock skew and jitter are 50 Ps and 25 Ps, respectively. Design a pipe-lined Carry-Ripple adder that can operate at the required data rate. All inputs and outputs should be registered.

FPGA Implementation Problem:

Q3) It is required to design and implement a 6-bit combination digital lock circuit. The circuit receives serial input combinations. If they match a 6-bit stored pattern, the lock is enabled. Also, the user can store a new pattern (i.e. re-program the lock). If 3 wrong combinations are entered in a row, the lock jams and need to be reset:

1. **Manually obtain the logic design of this lock (Data path and Control Unit),**
2. **Simulate your design using Xillinx design environment and verify its correctness**
3. **Implement the verified design on a Spartan (100K) FPGA prototyping board and test it to verify its correct operation. A demo on Sunday, 28th of March will be required.**