CSE670, Dr. Muhammad Elrabaa
Assignment #2

Theoretical Problems (Due 12/4/2004):

Q1) Implement the following function using a 4-input LUT and minimum # of 2-1 MUXs:

$$F = A + B \cdot C + D \cdot E$$

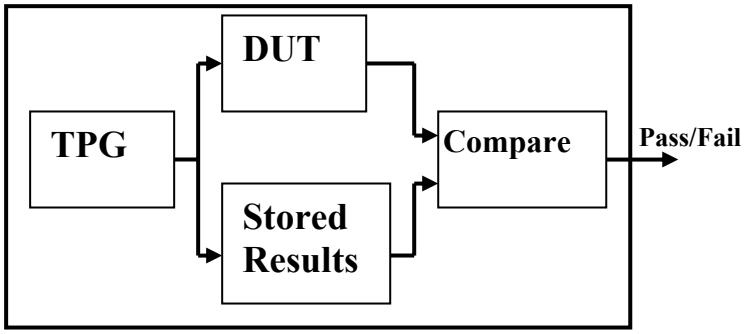
Q2) Using devices data sheets (for logic block architecture and timing models) estimate the number of Logic Blocks and I/O Blocks required to implement your Pipelined Adder (from assignment 1) and estimate the maximum clock frequency and pin-to-pin delays for the following FPGAs/CPLDs:

- **ACT3 (A1425A)**
- **Altera's MAX3000A (EPM3128A)**
- **Altera's FLEX10KE (EPF10K130E)**

FPGA Implementation Problems (Due 19/4/2004):

Q3) Implement your pipelined adder on the Spartan2 board. Using Xilinx tool suit find the # of used CLBs, IOBs, and estimate the maximum frequency of operation. Also devise a method for at-speed testing of your design.

Hint: Add a testing fixture on the FPGA with a single output indicating weather the design pass or failed the at-speed test.



Q4) Implement a regular version of your adder (not pipelined) and devise a method to measure the pin-to-pin delay and compare it to the value obtained from Xilinx tool suit.

Hint: Cascade several instances of your design such that the pin-to-pin delays are measurable using our regular Oscilliscopes. Then measure the delay and divided by the number of instances to get the delay of a single instance.