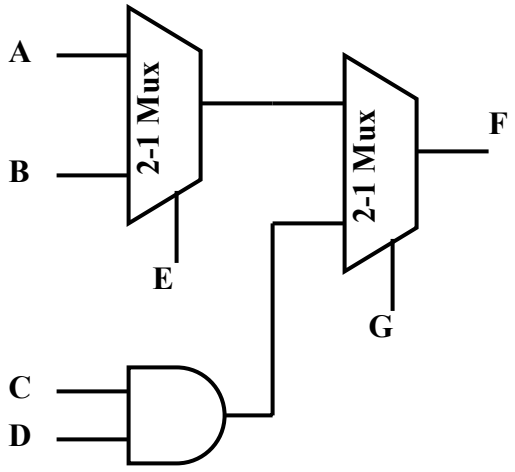
CSE670 Assignment #3
Due 26/5/2004

Q1) The figure below shows a Mux-based Logic Block:

1. Write the Boolean expression of the output F and estimate the number of possible functions that can be implemented with this LB.
2. Show the BDD of the LB
3. Show, using BDD and stuck-at-fault models, the technology mapping of the function **W** to this LB:

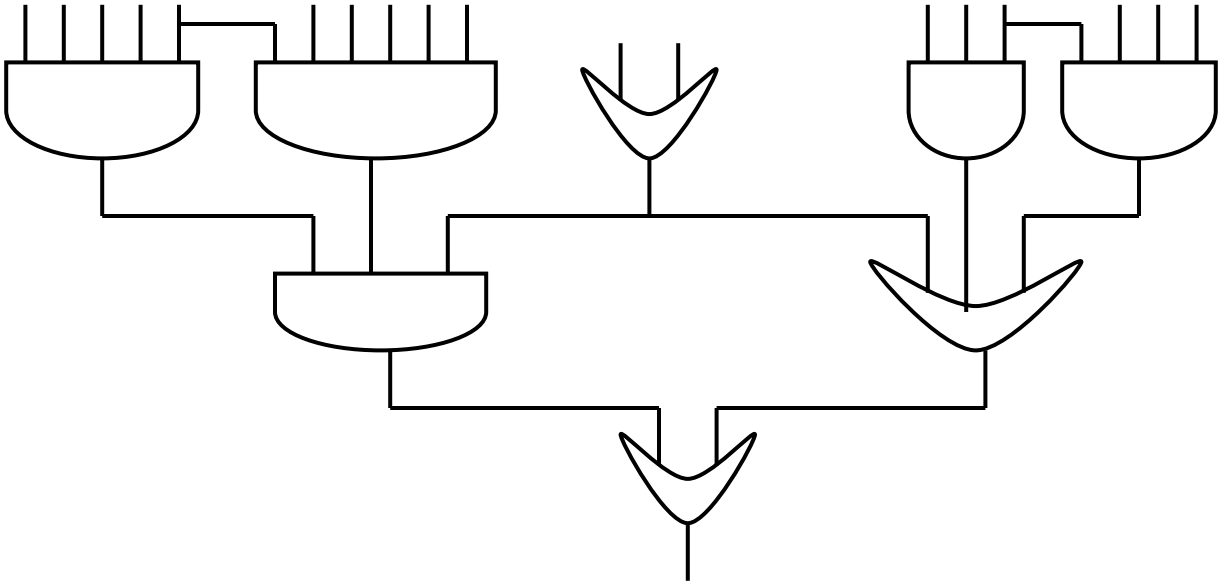
$$W = X \cdot Z + \overline{Y}$$



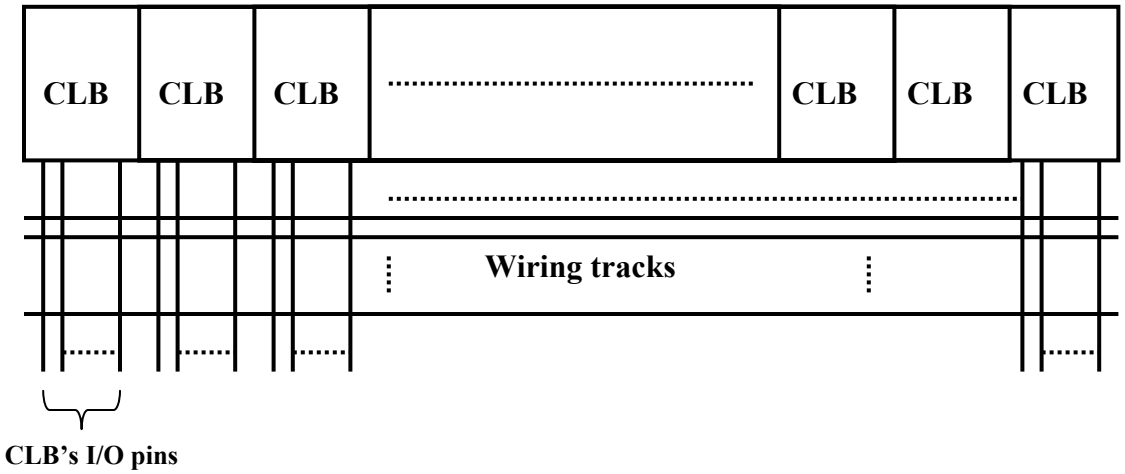
Q2) The figure below shows a logic network resulting from logic synthesis. Using the Chortle-crf algorithm:

1. Map this network to a minimum number of 4 I/P LUTs
2. Map this network to a minimum number of 6 I/P LUTs
3. Assuming a one-dimensional placement of these LUTs (i.e. row-based FPGA) , as shown below, estimate the minimum number of wiring tracks required for the 4-LUTs assuming:
   a. Fully-segmented tracks
   b. 4-segment tracks (each segment spans 4 LUTs)

   For the two above cases, show your actual placement and routing of the LUTs.



The synthesized logic network



The assumed FPGA architecture