Multiemitter BiCMOS CML Circuits

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Abstract—**New BiCMOS current-mode logic (CML) circuits employing multiemitter devices are proposed. They perform logic functions in addition to conversion from CMOS to CML (or ECL). Their transient behavior was analyzed, and their delay expressions were obtained and verified using HSPICE [6]. These expressions were used to optimize their design. Their performance is compared with other BiCMOS CML circuits with similar functionality.**

Nomenclature

β	Bipolar gain.
τ_F	Bipolar transit time.
C_{be}	Base-emitter junction capacitance.
C_{jc}	Collector junction capacitance.
C_{cm}	Miller's capacitance at the collector.
C_{js}	Collector–substrate junction capacitance.
C_{gs}	Gate–source capacitance in the linear region in the MOS HSPICE transient model.
C_{gd}	Gate–drain capacitance in the linear region in the MOS HSPICE transient model.
C_D	Source/drain depletion capacitance.
C_{ovl}	MOS overlap capacitance.
C_e	Capacitance at the common emitter node, $C_e = C_D + C_{ovl} + C_{be}$.
C_L	Load capacitance.
V_{th}	MOS threshold voltage.
V_s	Output voltage swing.
V_{ref}	Reference voltage.
V_{BE}	Base-emitter junction voltage of a turned-on bipolar.
$I_{D\text{sat}}$	MOS saturation current.
ΔQ_{gd}	Channel charge supplied by the drain node after the MOS enters the linear region.
ΔQ_{sd}	Channel charge supplied by the source node after the MOS enters the linear region.
I_{SDf}	MOS drain current when $V_{SG} = V_{DD}$ and the drain voltage is $V_{\text{ref}} - V_{BE}$.
r	Portion (percentage) of input transition where the MOS device at the input is in strong inversion.
V_T	Thermal voltage, $V_T \approx 26$ mV.

Manuscript received March 7, 1991; revised November 1, 1991. This work was supported in part by NSERC, ITRC, and MICRONET research grants.

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IEEE Log Number 9105978.

I. Introduction

OPTIMAL performance of large digital systems requires the use of CMOS, BiCMOS, and CML (or ECL) logic: CMOS for low-power densed logic and on-chip memories with BiCMOS gates as buffers and sense amplifiers, and the faster CML (or ECL) logic for implementing critical paths. Hence, it is necessary to have fast conversion logic to convert signals from CMOS (or BiCMOS) levels to CML level and vice versa. This paper deals with CMOS/CML conversion circuits.

Conversion circuits have been proposed and reported [1], [2] with speeds comparable to that of CML. Two of these circuits are considered for comparison. They can perform logic functions with mixed CMOS/CML inputs. However, they consume large static power and silicon area. Moreover, these circuits suffer in performance at reduced voltage supplies [1]. A new set of conversion circuits using merged BiCMOS structures with multiemitter bipolar transistors are proposed. Their operation, transient analysis, design, and a comparison between them and the existing circuits with similar functionality in terms of speed, power, area, and low-voltage operation are presented.

II. Conventional CMOS/CML Conversion Circuits

Two series-gated circuits are considered in this section—one with a conventional CMOS/CML translator (Fig. 1(a)) and one with a merged current switch logic (MCSL) [1] (Fig. 1(b)). The CMOS/CML translator operation was analyzed in [3], and analytical delay expressions were given. A drawback of this circuit is that, when the output of the CMOS gate at the CML input is rising, the CML part will only start to switch when this voltage approaches V_{ref}, which is less than V_{DD} by $V_s/2$. Thus, most of the rise time of the CMOS gate is added to the total gate delay. The MCSL has a better performance because it begins switching after a smaller change in the input; however, it suffers from performance degradation at low levels of supply voltage [1]. Moreover, the number of levels of series gated (stacked) CML gates for both circuits is limited by the supply voltage.

III. Multiemitter BiCMOS CML Circuits

Two new types of circuits are proposed to overcome the limitations of the above circuits. One is the low-power multiemitter merged MOS/bipolar CML (low-power M^3BiCML) of Fig. 1(c), and the second is the multiemitter merged MOS/bipolar CML (M^3BiCML) of Fig. 1(d).

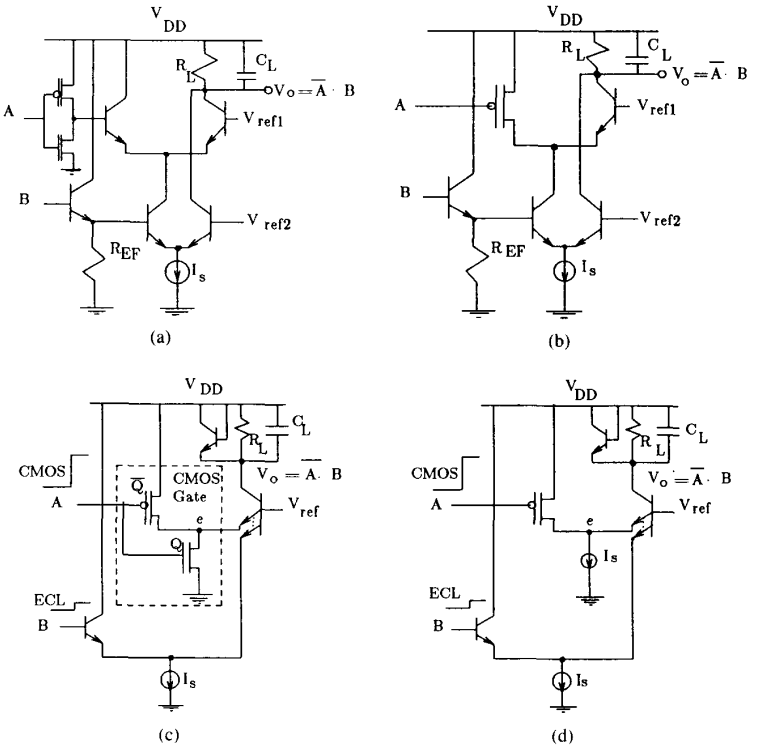

Fig. 1. Circuits diagrams of (a) conventional BiCMOS CMOS/CML translator, (b) the merged current switch gate, (c) low-power multiemitter merged MOS/bipolar CML, and (d) multiemitter merged MOS/bipolar CML. The diode-connected transistors are used to limit the output voltage swing.

A. Low-Power M^3BiCML

This circuit is composed of a conventional CML with a CML input, and a merged BiCMOS CML with a CMOS input. An NMOS transistor Q is acting as a current source when the A input is high. The channel width of Q is adjusted to the required value of current, which is the same as I_s in the CML part, and R_L is chosen to give the desired voltage swing. For equal probability of the two states (ZERO and ONE) of the input A, the merged part will draw power for only half the time. Hence, the average static power dissipated in this part is

$$P_{\text{ave}} = 0.5\, I_s V_{DD}.$$

The voltage swing at the emitter of the merged part (node e) is small ($V_{DD} - (V_{\text{ref}} - V_{BE})$). As it is shown later, a portion of this circuit delay is proportional to this voltage swing. A faster version of this circuit results if the positions of the NMOS (Q) and the PMOS ($\bar{Q}$) devices are interchanged since the voltage swing at node e would be reduced by V_{th}. The resulting circuit is called noninverting LPM^{3}BiCML.

Using multiemitter devices enables the implementation of more complex functions (or handling more inputs) at lower voltage supplies since no series gating is required [8]. The output capacitance is smaller than that of the conventional series-gated circuits since the collector area (and hence capacitance) of the multiemitter bipolar is smaller than the sum of the collector area of two bipolar transistors. The delay of the CML part was reported in many papers [4], [5]. The delay of the merged BiCMOS part is analyzed next. The input is assumed to be a voltage step rising (or falling) in a time $t_{\text{rise/fall}}$ (50 ps in this work), and the delay is measured from $t_{\text{rise/fall}}/2$ to the time the output reaches $V_{DD} - 0.5V_s$. The calculated results were compared to HSPICE simulations using the parameters in Table I.

1) Rise-Time Analysis: As the input decreases, the drain current of Q decreases, and by the end of t_{fall} this current and the emitter current of the bipolar transistor would have fallen to zero. Assuming t_{fall} is small enough, most of the base charge of the bipolar remains unchanged. This charge is then removed through diffusion in a time of the order of τ_F. Meanwhile, the collector current becomes zero and the output node capacitance C_o is charged to $V_{DD} - 0.5V_s$ in $0.7R_L C_o$, $C_o = C_L + C_{cm} + C_{js}$, and $C_{cm} = 2C_{jc}$ [4]. Thus, the rise time is given by

$$T_r = 0.5t_{\text{fall}} + \tau_F + 0.7R_L C_o. \tag{1}$$

2) Fall-Time Analysis: At the end of input change, the emitter node is still close to V_{DD}. Then it is discharged by $I_{D\text{sat}}$ of the NMOS transistor Q to about $V_{\text{ref}} - V_{BE}$, forcing the bipolar transistor to turn on in about τ_F. Finally, the output capacitance is discharged to $V_{DD} - 0.5V_s$ in $0.7R_L C_o$. Thus, the fall time is

TABLE I

	V_{th}	L_{eff}	$C_{S/D}$	C_{ovl}	Bipolar
NMOS	0.065 V	1 μm	4E-4 F/m	2E-10 F/m	G_{js} = 7.5 fF C_{js} = 31 fF
PMOS	−0.95 V	1 μm	5E-4 F/m	2E-10 F/m	C_{bc} = 7 fF τ_F = 6 ps
	V_{DD} = 5 V	V_s = 0.8 V	$V_{BE(on)}$ = 0.83 V		R_B = 200 β = 100

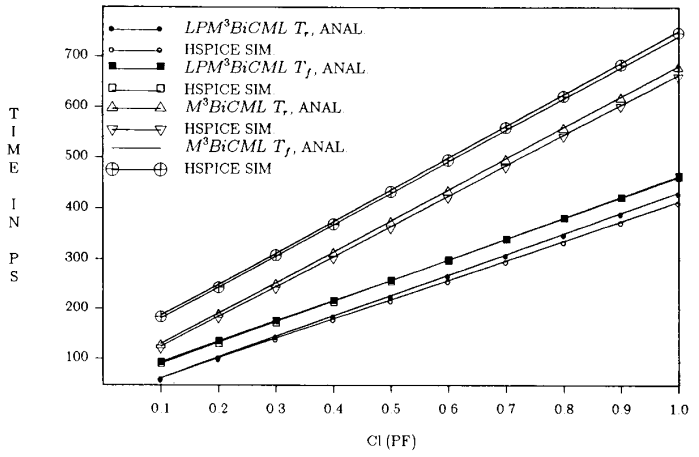

Fig. 2. The calculated and simulated rise and fall times of the new circuits.

$$T_F = 0.5t_{\text{rise}} + C_e[V_{DD} - (V_{\text{ref}} - V_{\text{BE}})]/I_{D\text{sat}} + \tau_F + 0.7R_L C_o. \quad (2)$$

A comparison between the above expressions and HSPICE is shown in Fig. 2. The total average delay is $0.5(T_R + T_F)$.

As can be seen from the above expressions for the rise and fall times, the PMOS width should be minimum (and satisfying the noise margins) to minimize C_e.

B. The M³BiCML

The M³BiCML circuit of Fig. 1(d) consists of a CML and a merged BiCMOS CML. The merged part is the same as the MCSL reported in [1]. The M³BiCML consumes more power than the LPM³BiCML. However, it has a superior ability to achieve more complex functions in smaller area at low power supplies since the current source is implemented by a bipolar transistor not a MOS transistor. Moreover, series gating is possible, giving the designer more freedom. The delay of the merged part is analyzed next.

1) Rise-Time Analysis: The rise time is divided into three times. The first time is the time required for the MOS device to turn on (during input transition) while the emitter current increases to $I_e(0)$, approximated as follows:

$$I_e(0) = I_s + 2(\Delta Q_{gd} - \Delta Q_{sd})/t_{\text{fall}} \quad (3)$$

where $\Delta Q_{gd} = C_{gd}\Delta V_{gd}$, ΔV_{gd} is the change in gate-to-drain voltage, and $\Delta Q_{sd} = 0.5rI_{SDf}t_{\text{fall}}$.

In the second time, V_e increases by about $4V_T$, and the emitter current becomes zero. These changes can be approximated to be linear and occur in a time t_{r1}:

$$t_{r1} = \frac{4V_T C_e + \tau_F I_e(0)}{I_{SD\text{ave}} - I_s} \quad (4)$$

where $I_{SD\text{ave}}$ is the average drain current during this time.

The final time is the RC charging of the output. Thus, the total rise time is

$$T_r = 0.5t_{\text{fall}} + t_{r1} + 0.7R_L C_o. \quad (5)$$

2) Fall-Time Analysis: By the end of the input transition, the PMOS is turned off. However, the channel charge causes the emitter node voltage to rise by ΔV_e. Since the drain current of the short-channel PMOS is approximately linear with V_{SG} (for $V_{SG} > V_{th}$) [7], it is linear with time. Hence, ΔV_e is approximated as

$$\Delta V_e = \frac{\Delta V_{gd} C_{gd} - t_{\text{rise}} I_s(1 - 0.5r)}{C_e}. \quad (6)$$

Next, the emitter node is discharged to $V_{\text{ref}} - V_{BE}$ in t_{dis}:

$$t_{dis} = C_e[V_{ei} - (V_{\text{ref}} - V_{BE})]/I_s \quad (7)$$

where V_{ei} is the voltage at the emitter node at the end of the input transition (including ΔV_e). Finally, the bipolar transistor turns on in about τ_F and the output capacitance is discharged in $0.7R_L C_o$. The total fall time is therefore

$$T_f = 0.5t_{\text{rise}} + t_{dis} + \tau_F + 0.7R_L C_o. \quad (8)$$

Comparisons between the above expressions of the rise

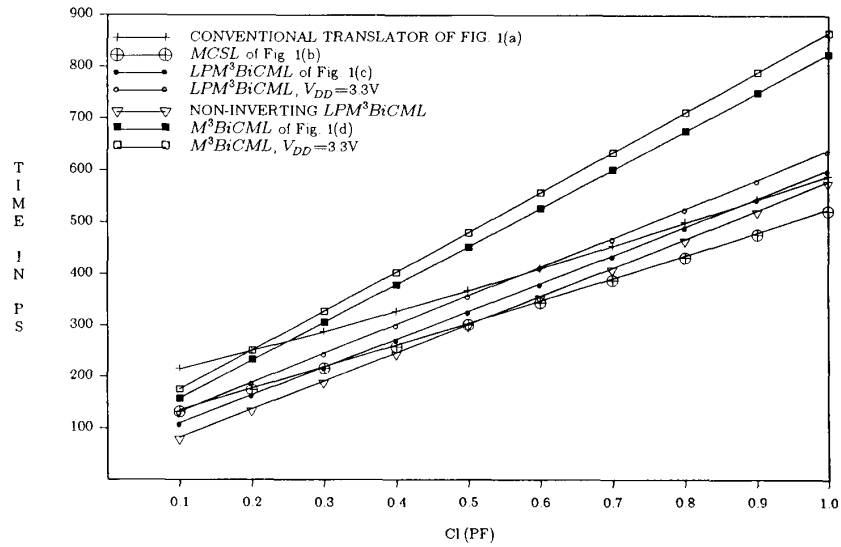

Fig. 3. The simulated average delays versus load capacitance for V_{DD} = 5 V except as indicated.

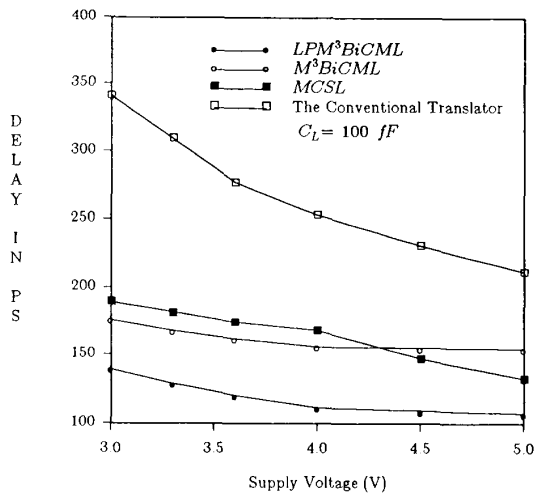

Fig. 4. The delays of the four circuits versus the supply voltage.

TABLE II

	LPM³BiCML	M³BiCML	Conv. Trans.	MCSL
Power (mW)	7.0	6.75	6.8	6.8
Area (normalized)	1	1.32	2.27	1.83
Delay (ps)	110	157.2	214	135.3
Delay-Power Product (PJ)	0.77	1.06	1.46	0.92

and fall times and HSPICE simulations are shown in Fig. 2. The total delay is $0.5(T_r + T_f)$.

The rise time is independent of the PMOS width (W_P), however, the fall time has a term (t_{dis}) that increases with W_P. Thus, W_P should be kept at a minimum value that satisfies the noise margin requirements. The emitter's areas (as in previous circuits) are also set to a minimum to avoid high-level injection effects and to minimize the parasitic capacitances [4].

IV. Results and Comparison

The average delays of the circuits described in this paper were measured as a function of load capacitance using HSPICE for the same level of power and are shown in

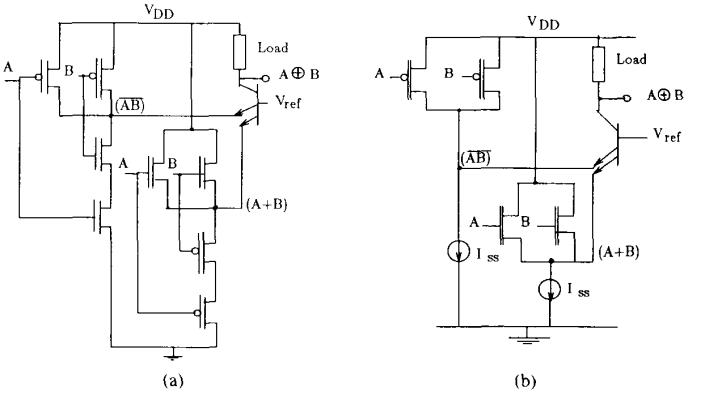

Fig. 5. XOR implementations using (a) LPM^{3}BiCML structure, and (b) M^{3}BiCML structure.

Fig. 3. The LPM^{3}BiCML and the noninverting LPM^{3}BiCML have the lowest delays for moderate values of load capacitance most likely to be encountered in a critical path. The delays of the new circuits under reduced supply voltage (3.3 V) do not increase significantly. Also, the delays of the four circuits as a function of the supply voltage are shown in Fig. 4, where it is clear that the new proposed circuits have a superior performance under lower supply voltages. Table II shows the relative area of each circuit, along with the delay, power, and delay–power product for a load capacitance of 0.1 pF. LPM^{3}BiCML and M^{3}BiCML circuits offer a powerful logic element and can implement complex logic functions at lower supply voltages, and an example of an XOR implementation is shown in Fig. 5.

V. Conclusion

New merged BiCMOS CML circuits are proposed. They utilize multiemitter BJT's instead of series gating to minimize the limitations imposed by lower supply voltage. Analytical expressions of their delays that can be used to optimize their design are obtained. They offer higher speed at the same power level for moderate load capacitances and up to 50% saving in area. Their performances do not degrade with the scaling down of the supply voltage. The use of multiemitter bipolar transistors instead of series gating enhances their logic functions' implementation capability and makes them adaptable to low supply voltage operation.

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