COE 205, Term 032

Computer Organization & Assembly Programming

Quiz# 2 (22/03/04)

Student Name: Key Solution **ID:** **Section:**

Question 1: Given the following declaration in the logical data segment**:**

```
.data
        X       DB      2 DUP (34H)
        Y       DW      2 DUP (?)
        M       EQU     234H
        W       DB      2  DUP (3, 2 DUP(0))
        Z       DW      0EFA2H
```

Show how these values would be represented in memory, if we suppose that data is put in memory starting from address: 2000 H

Variable	Address	Content	Variable	Address	Content
X	2000	34		2007	0
	2001	34		2008	0
Y	2002	?		2009	3
	2003	?		200A	0
	2004	?		200B	0
	2005	?		200C	A2
W	2006	3		200D	EF

Question 2: Given the following register contents**:**

AX = F2E9H BX = 0000H CX = 08A0H DX = F1E0H
SI = 0006H DI = 0010H BP = C2E1H SP = 1330H
DS = 1EC0H ES = 2FF4H CS = 1EC0H SS = A345H
IP = E731H

A – Calculate the physical address of the top of the stack?

PA = SS x 10H + SP = A3450 + 1330 = A4780H

B - Calculate the starting and ending physical addresses of the data, code stack and extra segments. Indicate whether the segments are disjoint or overlapping?. Indicate also the overlap is partial or total?.

Segment	Pointing Register	Starting Physical Address	Ending Physical Address
Data	DS	1EC00	1EC00 + FFFF = 2EBFFH
Code	CS	1EC00	1EC00 + FFFF = 2EBFFH
Stack	SS	A3450	A3450 + FFFF = B344FH
Extra	ES	2FF40	2FF40 + FFFF = 3FF3FH

- DS and CS are totally overlapping
- All other cases are totally disjoint

C – Indicate what (source) addressing modes are used in the following instructions?
Note: indicate if any of the instructions syntax is incorrect. In that case you don't have to calculate the physical address

	Instruction	T/F	Addressing Mode	Physical Address Calculation
1	MOV AX, [BX+2]	T	Based	DSx10h + BX + 2
2	SUB SI, [BX+SI]	T	Based Indexed	DSx10h + BX + SI
3	SBB SI, [BX + Z]	T	Based	DSx10h + BX + Offset Z
4	MOV [BX+3], M	T	Immediate	No physical address
5	ADD [SI+6], BX	T	Register	No physical address
6	ADD X, Y[BX]	F	Both operands in memory	
7	MOV AX, X+2	F	Incompatible Operands	
8	ADC DX, Z[BX]	T	Register Indirect	DSx10h + BX + Offset Z