King Fahd University of Petroleum and Minerals
College of Computer Sciences and Engineering
Department of Computer Engineering

COE 202 Fundamentals of Computer Engineering (3-0-3)

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Term: 061 (1st term 2006–2007)
Day & Time: SMW 10:00 AM – 10:50 AM
Location: 24-236A
Prequisite: PHSY 102 (General Physics II)
Textbook: *Logic and Computer Design Fundamentals*, Morris Mano and Charles Kime, Third Edition, Prentice Hall International, 2004.
Office Hours: SMW 12:00 PM – 01:00 PM (or by appointment)
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Tentative Grading Policy:

- Quizzes & Homeworks **20%** (Each quiz and homework may carry a different weight)
- Major Exam I **20%** (Saturday November 04, 2006 from 07:00 PM to 09:00 PM)
- Major Exam II **25%** (Saturday December 09, 2006 from 07:00 PM to 09:00 PM)
- Final Exam **35%** (***Comprehensive***)

IMPORTANT NOTES:

- All KFUPM regulations and standards will be enforced. Attendance will be checked each class. The KFUPM rule pertaining to a DN grade will be strictly enforced (i.e. > **9 absences** will result in a DN grade). *Check your university e-mail, both KFUPM and CCSE, regularly for warnings regarding your absences.*
- If you are late to the class for more than 5 minutes (i.e. arrive after 10:05 AM), you will **NOT be allowed to enter** the classroom and you will be considered absent for that class.
- Only university approved/certified excuses will be accepted, and should be presented **no later than 1 week** after absence.
- Homeworks are to be submitted **in class** on the due date during the class period. Late homeworks will **NOT be accepted**.
- You have 48 hours to object to the grade of a homework, a quiz, or a major exam from the end of the class time in which the graded papers have been distributed back. If for some reason you cannot contact me within this period, send me an email requesting an appointment. The email should be sent within the 48-hour time period.
- **NO make up exams**. ALL homeworks and quizzes will be counted towards your grade.
- Final exam is **comprehensive**.
- General guidelines for grades:

Range	**≥ 90 and ≤ 100**	**≥ 80 and < 90**	**≥ 70 and < 80**	**≥ 60 and < 70**	**< 60**
Minimum Grade	**A**	**B**	**C**	**D**	**F**

Tentative schedule:

Week	Class	Subject	Textbook Section
		Number System and Codes	
1	1	Introduction. Information processing and representation. Digital vs Analog	1.1
	2	Number Systems. Binary, octal and hexadecimal numbers	1.2, 1.3
2	3	Number base conversion (Dec to Bin, Oct, and Hex, General)	1.3
	4	Conversion (Bin, OCT, Hex), Binary & other System Arithmetic	1.3
	5	Signed Binary Number representation, Signed Mag, R's &(R-1)'s Complement	Handout
3	6	Signed Binary Addition and Subtraction. R's &(R-1)'s Complement	Handout
	7	Signed Binary Addition and Subtraction. R's &(R-1)'s Complement	Handout
	8	Codes. BCD, Excess-3, Parity Bits, ASCII & Uni-Codes	1.4, 1.5, Handout
		Binary Logic & Gates	
4	9	Binary logic and gates, Boolean Algebra, Basic identities of Boolean algebra.	2.1, 2.2
	10	Boolean functions, Algebraic manipulation, Complement of a function.	2.2
	11	Canonical & Standard forms, Minterms & Maxterms, Sum of products, Product of Sums.	2.3
5	12	***Map method of simplification***: Two-, Three-, and Four-variable K-Map.	2.4
	13	***Map method of simplification***: Five, and Six-variable K-Map.	Handout
6	14	***Map manipulation:*** Essential prime implicants, Nonessential prime implicants, Simplification procedure.	2.4
	15	Don't care conditions and Simplification.	2.5
	16	Universal gates; ***NAND and NOR gates:*** 2-level implementation.	2.6
7	17	***Multilevel NAND Circuits***.	2.6
	18	Exclusive-OR (XOR) and Equivalence (XNOR) gates, Parity generation and checking.	2.7
		Combinational Logic	
	19	Combinational Logic, Design procedure. BCD-to-Excess 3 code Conversion.	3.4
8	20	BCD-to-7 Segment Display. Half and Full Adders.	Partial 3.4, 3.8
	21	Design using MSI parts. Decoders, Decoder Expansion. Combinational Circuit implementation using decoders.	3.5
	22	Encoders & Priority Encoders *Magnitude Comparator*.	3.6, Handout
9	23	Multiplexers. Function Implementation using multiplexers, Demultiplexers	3.7
	24	***Binary Adders:*** 4-Bit Ripple Carry Adder, Carry Look-Ahead Adder, Binary Adder-Subtractor.	3.8, 3.10
	25	BCD Adder, Binary Multiplier.	3.11, 3.12
		Sequential Circuits	
10	26	***Sequential Circuits:*** Latches, SR and D-latch, Clocked latch.	4.1, 4.2
	27	***Flip-Flops:*** Master-Slave, Edge-Triggered. *Timing Diagrams*	4.3
11	28	***Flip-Flops Characteristic & Excitation Tables:*** D-FF, SR-FF, JK-FF, T-FF. ***Asynchronous/Direct Clear and Set Inputs***	4.3
	29	Setup, Hold, Enable times. Timing control and Clocks. Path delay constraints.	Handout
	30	***Sequential Circuit Design:*** Design procedure, Construction of state diagrams and state tables.	4.5
12	31	Designing with D-FFs. Designing with unused states.	4.6
	32	Designing with JK-FFs, Flip-Flop	4.7
	33	Sequential Circuit Design Examples.	
13	34	***Sequential Circuit Analysis:*** Input equations, State table.	4.4
		Registers & Counters	
	35	Registers, Registers with parallel load, Shift Registers.	5.2, 5.3
	36	Shift register with parallel load, Bi-directional shift register.	5.3
14	37	***Ripple Counters:*** Up-Down Counters. Synchronous Binary Counters: ***Counters with JK-FF, Counters with D-FF.***	5.4
	38	Serial & Parallel Counter, Up-Down Binary Counter, Binary Counter with Parallel Load.	5.5
	39	Other Counters: BCD Counter, Arbitrary Count Sequence.	5.5
		Memory & PLDs	
15	40	***Memory and Programmable Logic Devices:*** Read-Only Memory.	6.1, 6.7
	41	Combinational Circuit Implementation with ROM.	6.7
	42	Programmable logic array, Programmable array logic, Prog. logic devices, FPGAs	6.8, 6.9