Computer Aided Design of Digital Systems - COE572
Homework IV.
Date: Fall 2003.

Question 1.
In not more that one/two sentences, answer the following.

1. Why is Simulated Annealing called a non-deterministic algorithm?

2. What do you understand by the terms Metropolis Criterion, and, Cooling Schedule.

3. Explain the term "cooling schedule" as applied to Simulated Annealing.

4. Having implemented simulated annealing for your application, explain how you will choose the initial temperature and other constants.

5. What is the significance of the comparison below in the Simulated Annealing
$$(random < e^{-\Delta h/T})$$
where $\Delta h = (Cost(NewS) - Cost(S))$?

6. If you are to replace the exponential function $(e^{-\Delta h/T})$ by a linear function, what characteristic must this linear function have? (Illustrate with a figure).

7. Compare Simulated Annealing with genetic algorithm (not more than 3 or four significant differences).

   With respect to *Genetic Algorithm*, briefly answer the following questions.

8. What do you understand by 'survival of the fittest' and how and where is it applied?

9. What is the purpose of the Crossover operator?

10. What are the various points in the algorithm where non-determinism is introduced (give at least three)?

Question 2.
Consider a gate G, with negligible base delay (BD) located at origin (0,0) driving 5 other identical gates located at coordinates (5,10), (20,5), (25,40), 30,8) and (35,35) (all coordinates are in micrometers). Find the delay seen by the signal at the gate G. Make suitable assumptions. Your are given the following:

**a.** the input pin capacitance of the driven gates is 0.1 picoFarads,

**b.** the load factor of the driving gate G is 3 nSec/picoFarads,

**c.** the same material metal 1 ($m_1$) is used for both horizontal and vertical routing,

**d.** the width of the material metal 1 ($m_1$) is 3 $\mu$m, and

**e.** the capacitance per unit area of $m_1$ is 0.01 picoFarads/$\mu^2$.

State the technique you will use to estimate the length of the interconnect. (Hint: Delay seen by the signal driven by a gate is given by Base Delay + Load Factor * Capacitance).

Question 3.
You are required to find a solution to place the modules of the graph into slots. The number next to the gate indicates its size. You may use any technique to partition (even visual observation) but you must use terminal propagation to obtain the solution.
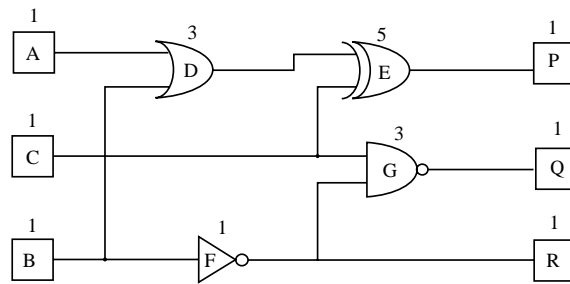


Figure 1: Circuit for Question 3.

Question 4.
The polish expression of a slicing floorplan is an elegant encoding expressed as a string of symbols. If you choose such a string as a chromosome, then what type of crossover(s) can you use in the genetic algorithm. Suggest at least two. Apply your crossover to the two strings given below (the point of crossover maybe around the middle of the chromosome):

$$P_1 = 53V24VH1V; P_2 = 12V3V4H5H$$

Suggest at least three mutation operators.

Question 5.
Given below is a graph whose nodes (12) represent gates of a circuit to be placed. Genetic algorithm is to be used for circuit placement. The encoding scheme (chromosome) for the initial placement given in Figure (b) can be represented by the following string.

$$l \ e \ a \ g \ b \ h \ d \ k \ f \ j \ c \ i$$

Answer the following questions:

1. What is the cost of the initial placement in terms of wirelength if 'semi-perimeter' method is used for estimation?

2. What is the resulting placement, if the initial configuration is crossed with the configuration (second parent) below using the partially mapped (PMX) and Order crossovers?

$$i \ j \ l \ c \ k \ a \ g \ b \ f \ d \ e \ h$$

Assume point of crossover to be after the $5^{th}$ gene.