Syllabus

COE 572: Computer Aided Design of Digital Systems (3-0-3)

Instructor: Sadiq M. Sait (14/254, TBA, Phone #1099/1900)

Catalog Description:

An up-to-date survey of design automation techniques for digital hardware designers. Digital design languages. System level simulation. Register-transfer-level description and simulation. Gate-level simulation. Partitioning, placement and routing for printed and integrated circuits. Fault simulation and test generation. Automated documentation. Integrated design systems. Hands-on experience on an actual design automation system.

Text Book:

'VLSI Physical Design Automation: Theory and Practice' by Sadiq M. Sait and Habib Youssef, World Scientific Publishers, Singapore/New-Jersey, USA, 1999 (Also published by McGraw-Hill Book Co., Europe, December 1995).

Additional Material:

'Iterative Computer Algorithms with Applications in Engineering (Solving Combinatorial Optimization Problems)' by Sadiq M. Sait and Habib Youssef, IEEE Computer Society Press, 1999, USA. (Also published by John-Wiley International, 2003).

Topics covered:

a. **Introduction to Design Automation.** Chapter 1 of the book describes all steps required to design digital systems. It also surveys and discusses current VLSI design methodologies and layout styles.

   This chapter motivates the student toward a study of Design Automation of Integrated Circuits. Layout is examined in the backdrop of the entire design automation process. Basic terminology is introduced, and the important sub-problems of layout are identified. The fact that many layout sub-problems are "hard" is brought out with illustrative examples.

b. **Partitioning for PCB and IC Design.** This material is covered in Chapter 2, Partitioning. The chapter concisely describes the partitioning problem and three of the most popular solution techniques, which are, Kernighan-Lin algorithm, Fiduccia-Mattheyses algorithm, and Simulated annealing approach.

c. **Modern Iterative Heuristics.** These heuristics, namely, simulated annealing, genetic algorithm, tabu search, stochastic evolution, and simulated evolution will be discussed as a major part of the course. Course projects will involve using these heuristics to solve some hard physical design and design automation problems.

d. **Floorplanning.** Chapter 3 formally defines the floorplanning problem and describes some techniques.

e. **Placement.** Chapter 4 of the book presents in detail the three most widely used placement techniques, that is, (1) Min-cut placement, (2) Simulated annealing approach, and (3) Force directed approach. Also Genetic Placement is fairly well described.

f. **Routing.** Chapters 5, 6, and 7, are dedicated to the topic of routing. All aspects of routing are addressed (grid routing, global routing, channel routing, and switchbox routing). For each routing sub-problem, popular algorithms are described and illustrated with examples.

g. **Other Aspects.** Chapters 8, 9 are dedicated to mask level aspects. Chapter 8 discusses the subject of silicon compilation and all aspects of automatic cell layout generation, that is, algorithms, optimization, etc., for three popular design styles (standard-cell layout, gate-matrix methodology, and PLAs). The 9th and final chapter briefly describes layout editors, and an important related problem, that is, layout compaction.

Grading Policy (To be discussed in class):

Major Examination I	20%
Major Examination II	25%
Term Project	25%
Final Written Examination	30%

List of Possible Projects:

1. Evolutionary Algorithms in Computer Aided Circuit Design.
2. Design Issues in Nanotechnology.
3. CAD for MEMS (Micro-Electro-Mechanical Systems).
4. Low Power Estimation Techniques in various phases of the VLSI Design Cycle.
5. Parallelizing general iterative techniques for solving Design Problems.
6. Ant Colony Optimization in System Design.
7. Study of Evolvable Hardware and their Applications.
8. Automation issues in Embedded Systems.