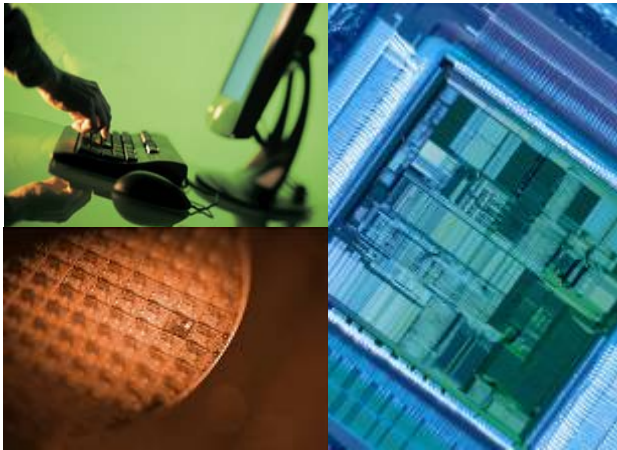


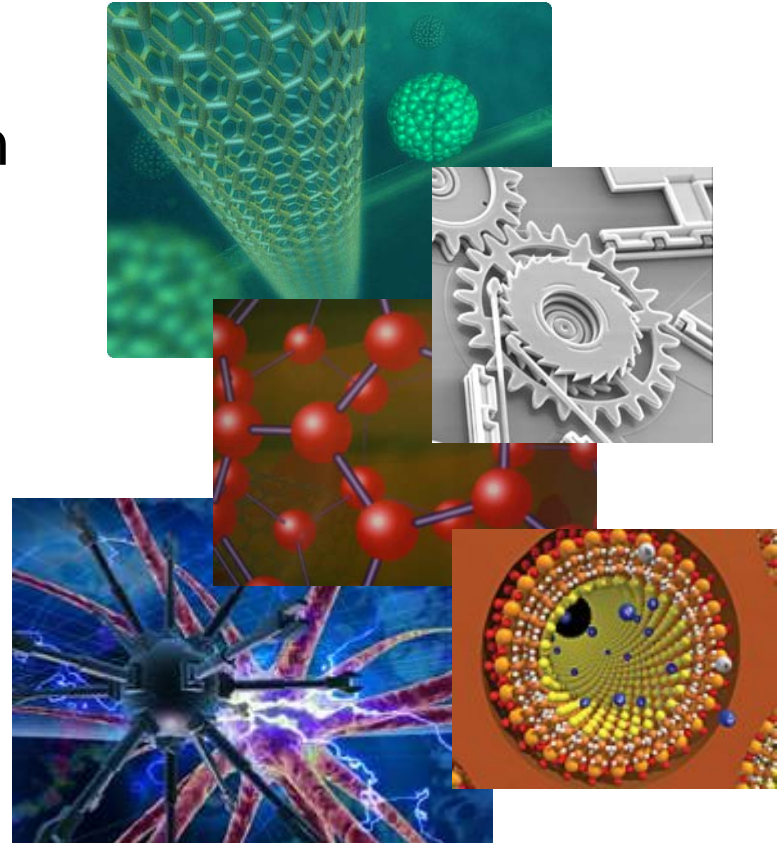
# Semiconductor & EDA Challenges in the Era of Nanotechnology



Rich Goldman  
Vice President,  
Strategic Market Development  
IEEE-GCC, Bahrain  
November 2007

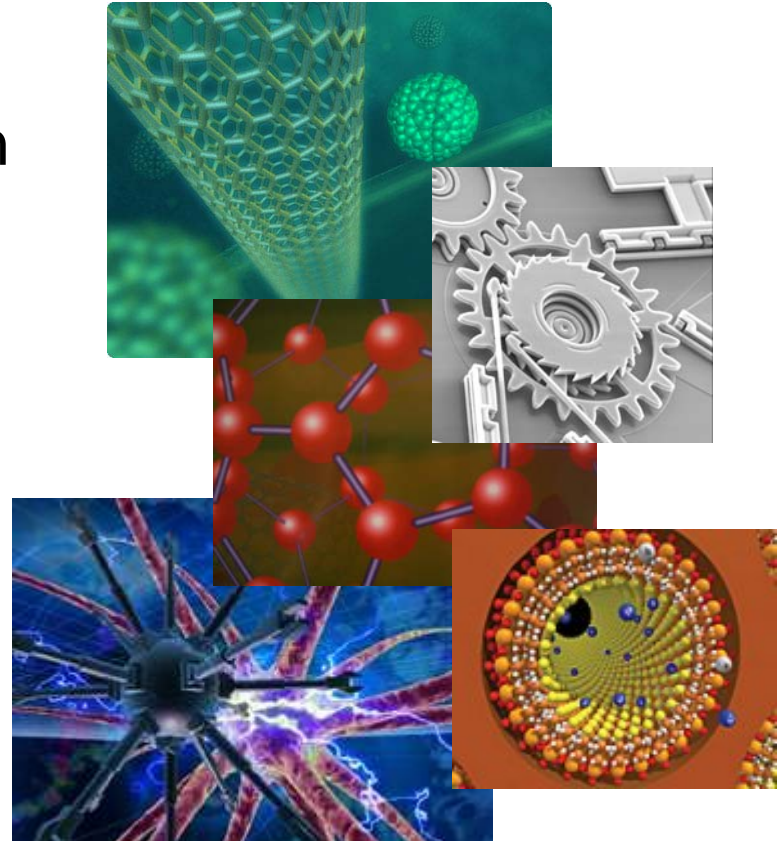
# Agenda

- What is Nanotechnology?
- Semiconductor Challenges in the Nanotechnology Age
- Implications for EDA
- Summary



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# What Nano IS, and what Nano is NOT

- Nano is **NOT** new
  - Romans-> gold ruby ~70nm diameter!!
- It is **NOT** an industry
  - It is a discipline utilized by many industries
- **Advanced Semiconductor Technology**  
**IS** the modeling, design, and manufacturing of structures, devices, and systems by manipulating and controlling sizes at nanometer scale to enable novel applications

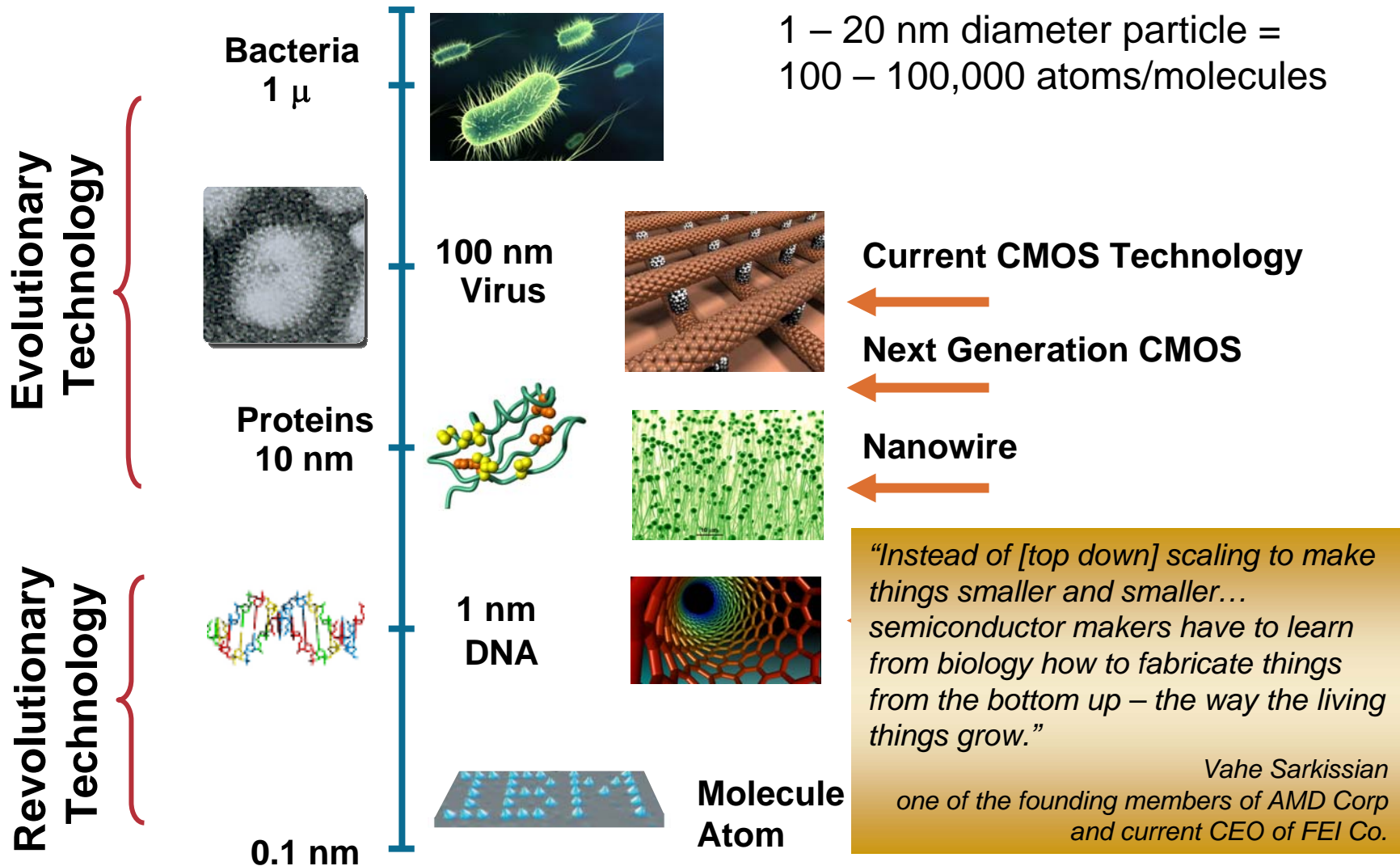


0.001% nano particles



Lycurgus cup  
4<sup>th</sup> century AD

# Size Matters!





# Milestones of “Modern” Nanotechnology

**1959:** Richard Feynman “there is plenty of room at the bottom”

**1974:** Norio Taniguchi coins the term nano-technology

**1981:** IBM researchers invent the Scanning Tunneling Microscope (STM)

**1986:** IBM researches invent the Atomic Force Microscope (AFM)

**1988:** Bell Laboratories discover quantum dots

**1989:** IBM researchers use STM to arrange 35 Xenon atoms and write IBM

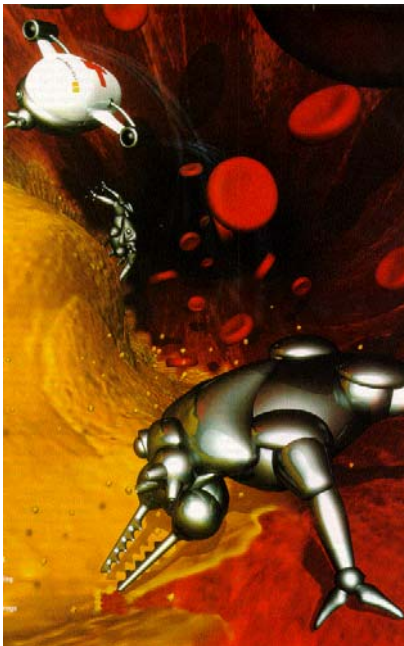
**1991:** NEC’s Sumio Iijima discovers the carbon nanotube

**1995:** Richard Smalley discovers the fullerene carbon nanotube

**2003:** IBM creates the world’s smallest solid-state light emitter

**What’s Next!**

**We are only at the beginning!**



# Applications of “Modern” Nanotechnology



Thursday, May 03, 2007

## Self-Assembly to Make Faster Chips

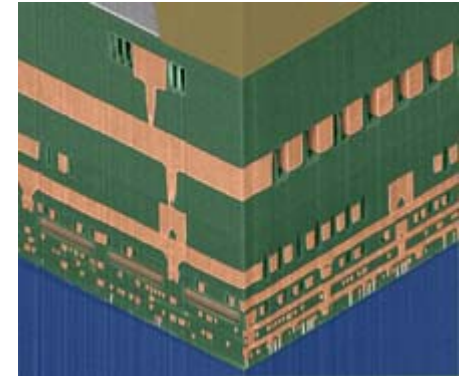
**IBM has developed a process for making speedier and more energy-efficient chips.**

By Kate Greene

The self-assembly of nanoscale structures, in which molecules arrange themselves in precise ways according to fundamental laws of physics, has long been a dream of chip designers. That's because it could be far cheaper to make ultrasmall precise features with self-assembly than with existing chip-making techniques. Now IBM researchers have taken a step toward using self-assembly in making future microprocessors.

The company has announced a novel process that uses self-assembly techniques to create air gaps that insulate wires in microprocessors. Early results show that these air-gap insulators can increase the speed of a chip by 35 percent or allow it to consume 15 percent less power than chips without the air-gap insulator. The company expects that the new process will be implemented in semiconductor facilities by 2009.

The new self-assembly approach ushers in to chip making an era of nanotechnology, says [Daniel Edelstein](#), IBM fellow and chief scientist for the self-assembly air-gap project. Importantly, Edelstein says, IBM's process is designed to be compatible with current manufacturing facilities and materials.



**Chips that make themselves:**  
This microprocessor cross section shows empty space in between the chip's copper wiring. Wires are usually insulated with a glasslike material, but IBM has used self-assembly techniques, which can be employed in chip-making facilities, to create air gaps that insulate the wires.

# Applications of “Modern” Nanotechnology

November 09, 2006

## Nanotechnology shown to remove arsenic from water



Scientists at [Rice University](#) in Houston have adapted nanotechnology to clean arsenic contaminated drinking water cheap and simple enough to use in developing countries such as Bangladesh, where 57 million people drink water from wells with dangerously high levels of arsenic.

The discovery emerged after tests with precision-engineered particles showed they were 100 to 1,000 times more effective at stripping toxic contaminants from water than existing filters.

The team of scientists, lead by Vicki Colvin, director of [Rice University's Centre for Biological and Environmental Nanotechnology](#), described in the journal *Science* today how nanoparticles of iron oxide, measuring 12 nanometres across - or 5,000 times smaller than the width of a human hair - could get arsenic in water below international safety thresholds, as [reported](#) by the [Guardian Unlimited, UK](#).

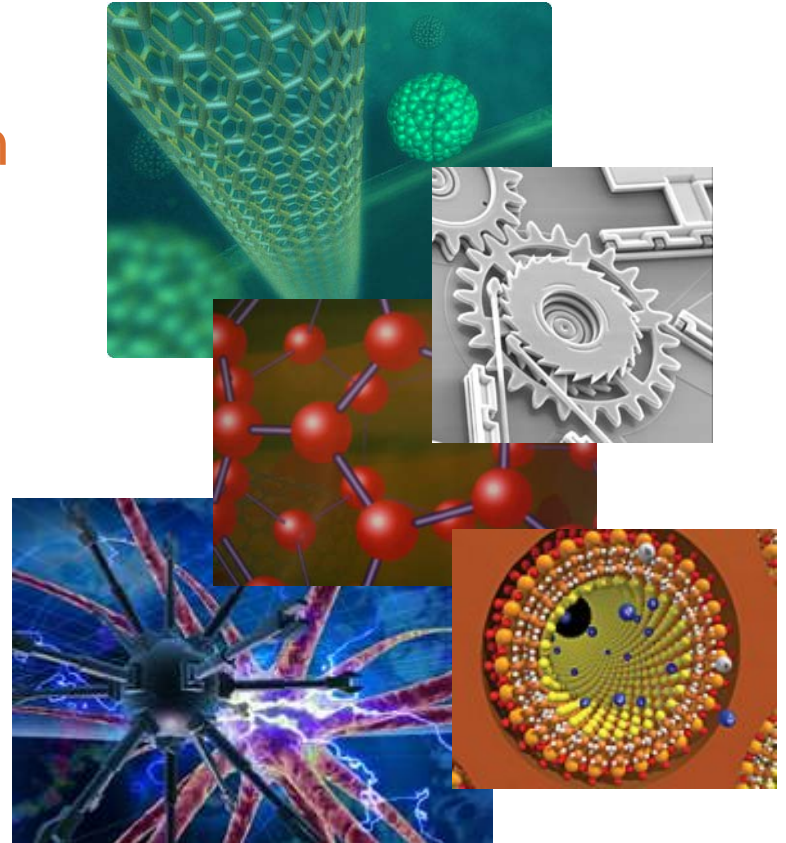


Arsenic binds easily to  $\text{Fe}_3\text{O}_4$  nanocrystals allowing it to be removed from drinking water when the ‘nano-rust’ is fished out of the solution by a low-field magnet.

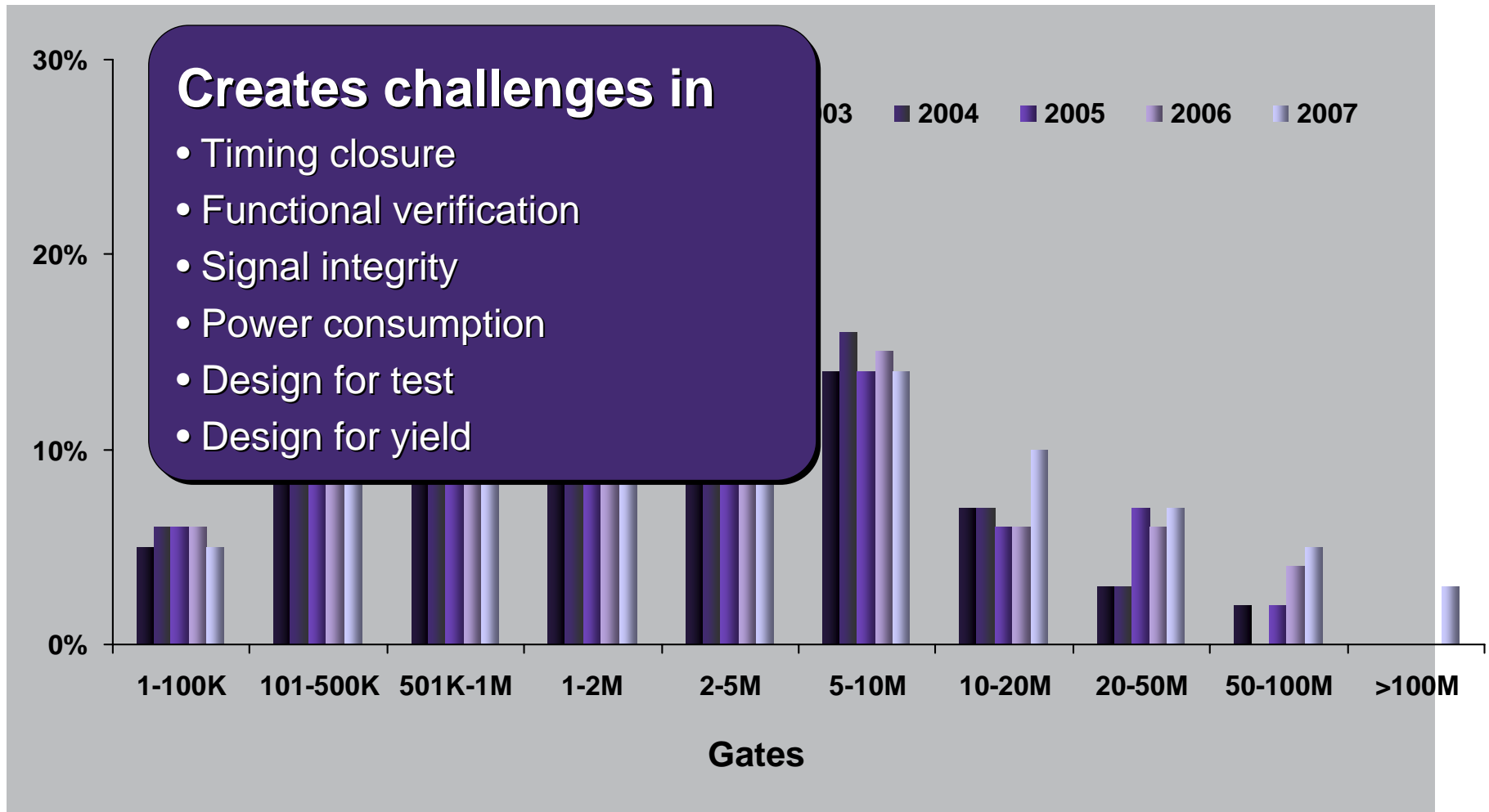


# Agenda

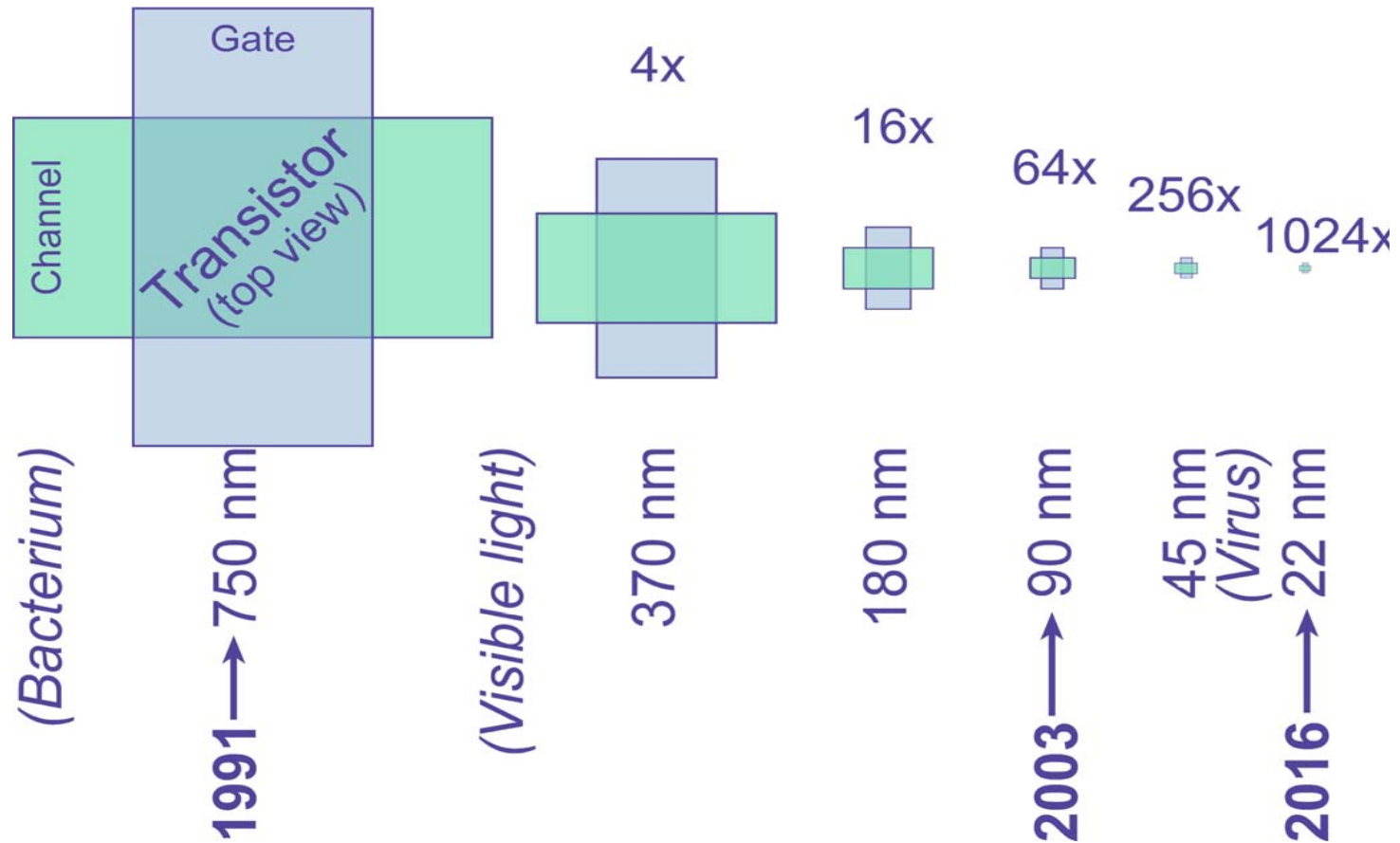
- What is Nanotechnology?
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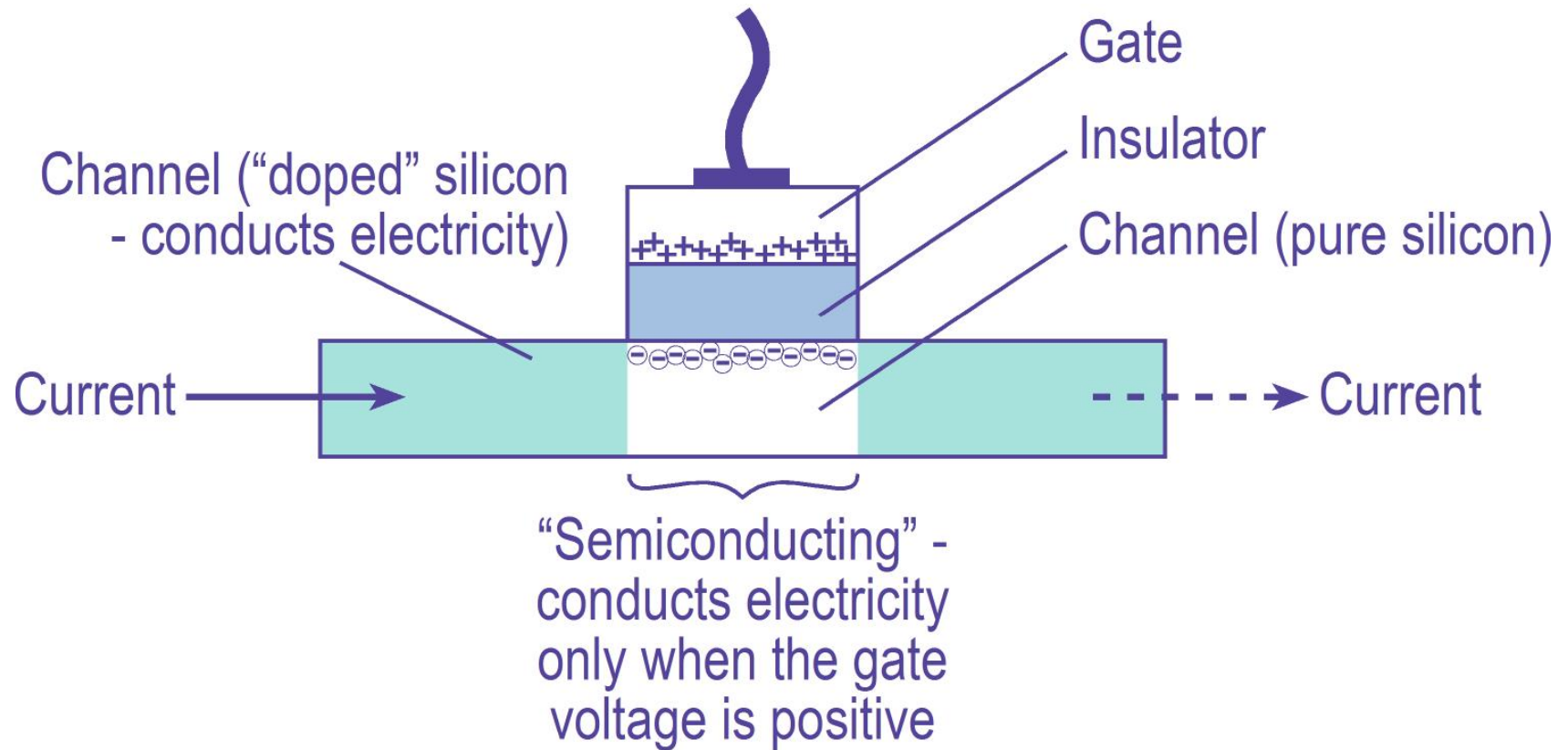
# Gate Count Exploding!



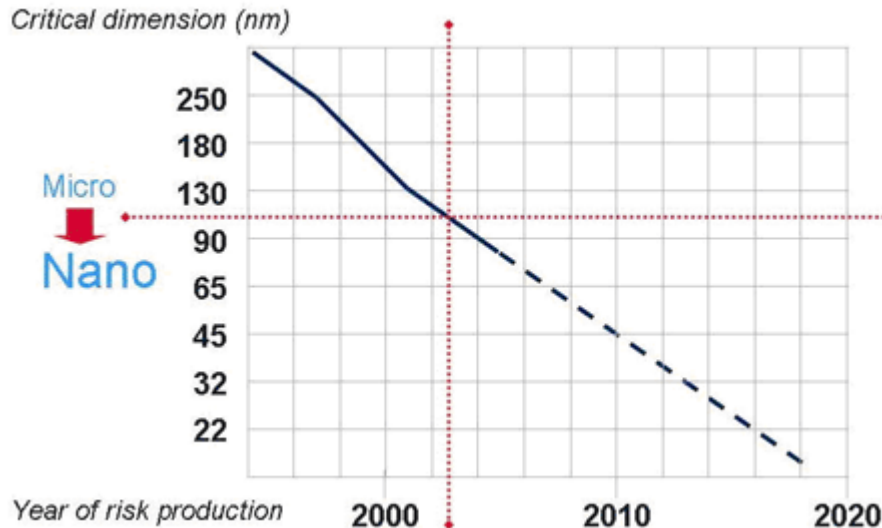
# Semiconductor State-of-the-Art



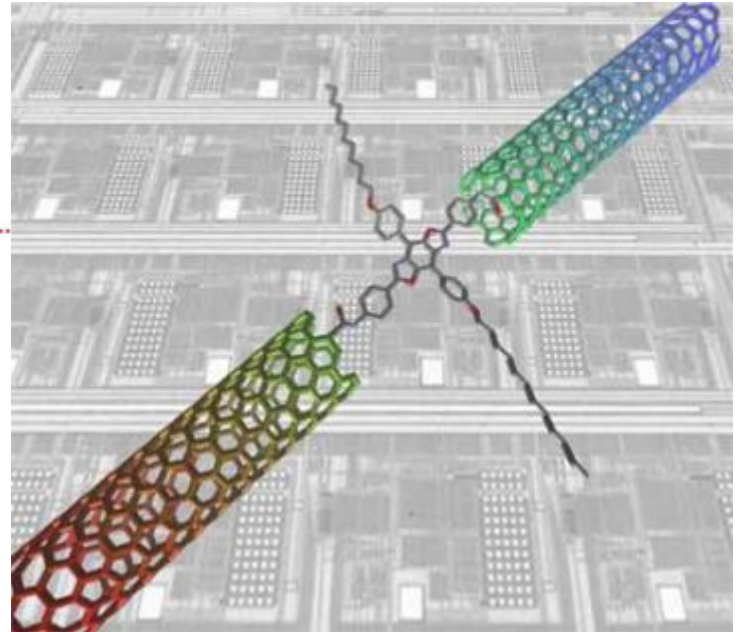
# CMOS Transistor: Is It Nanotechnology? Manipulating <100 nm particles?



# Moving Beyond CMOS to Molecular Electronics



*The International Technology Roadmap sees 32nm CMOS in production by 2015.*

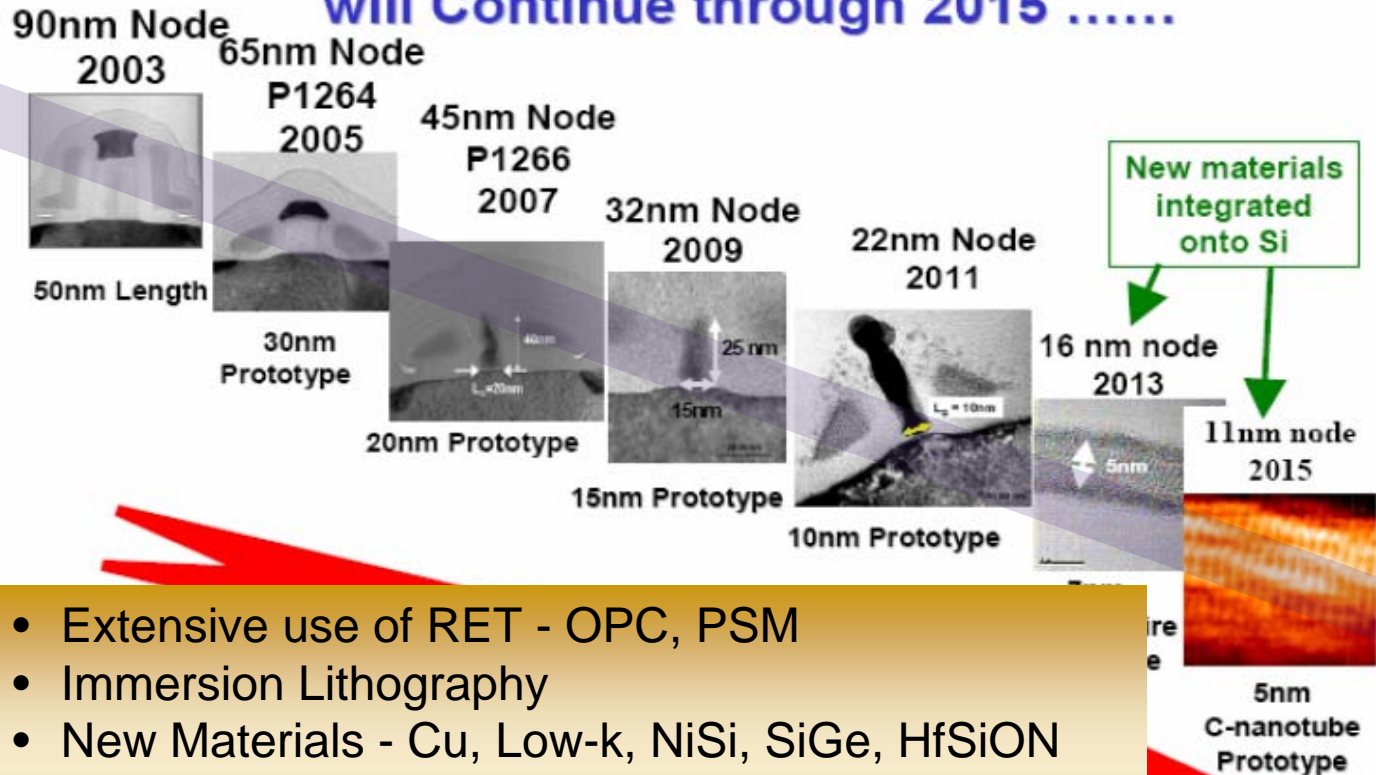


A digital rendering of two carbon nanotubes linked by a single organic molecule. Such arrangements are much smaller than the traditional integrated circuit. (Columbia University's Nanoscience Center)



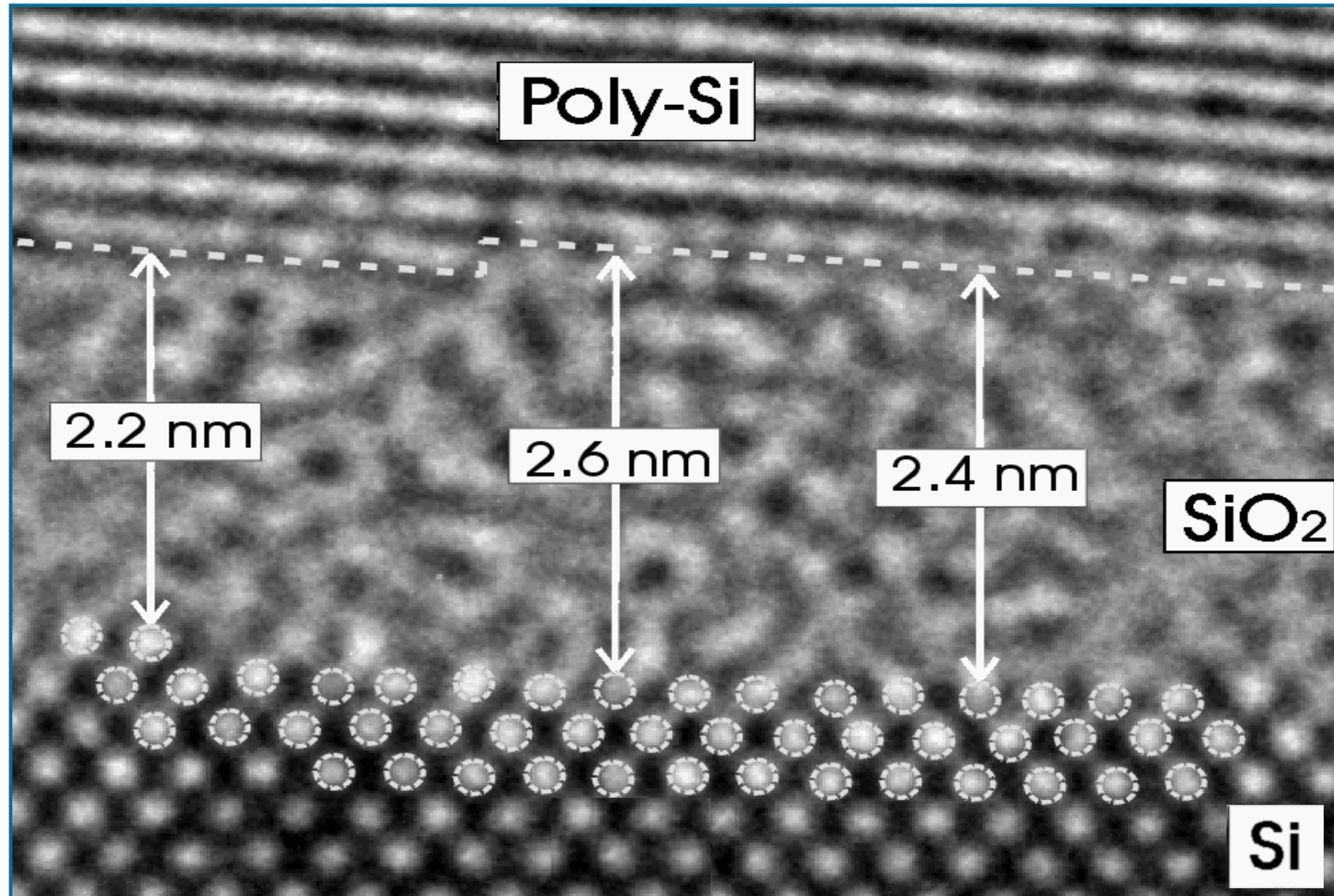
# Toward the Single Electron Transistor

## Silicon Transistor Scaling and Moore's Law will Continue through 2015 .....



- Extensive use of RET - OPC, PSM
- Immersion Lithography
- New Materials - Cu, Low-k, NiSi, SiGe, HfSiON
- New Device Types – FinFET, CNT
- Limits of Classical Scaling
- Increased Variation - Random, Systematic

# Nanometer Design: Atoms and Molecules Make the Difference



# Silicon: Out of Performance?

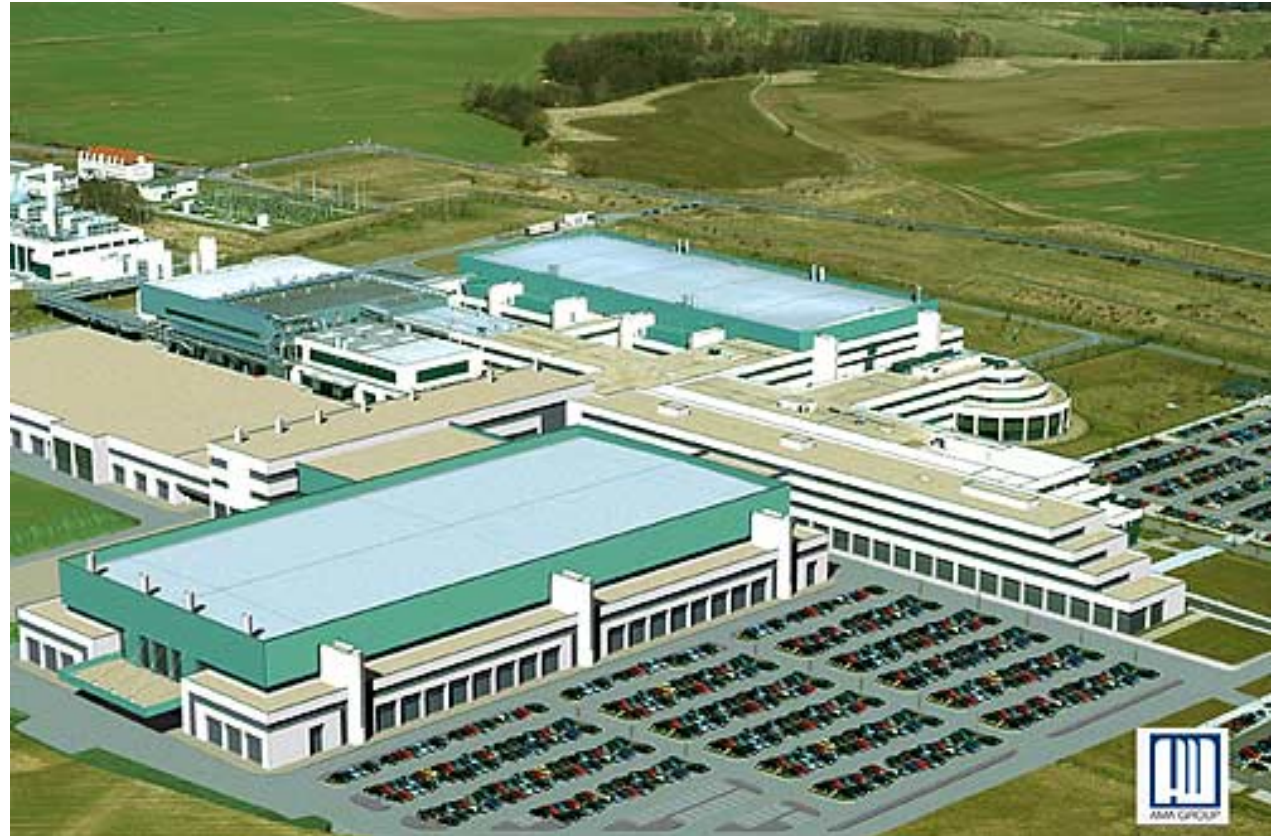
- Processing equipment too expensive
  - >\$3 billion per fab
- Top-down methods at limit
  - Features smaller than exposure wavelength
  - Non-uniformity of on-chip transistors
  - Processes no longer scale linearly
- Oxides too thin –just a few atoms
  - Leakage currents too high

*"We've now reached the point at which transistors are so small that our ability to keep shrinking them is facing some challenges. When we make them smaller, they're not automatically faster anymore."*

*Jeffrey Welser  
IBM Microelectronics Semiconductor  
Research and Development Center*

# Semiconductor Industry Investment

- Materials purification
- Lithography
- Materials science
- Precision process control
- Advanced microscope design
- ...and much more
- Key enablers for MEMS and nanotechnology

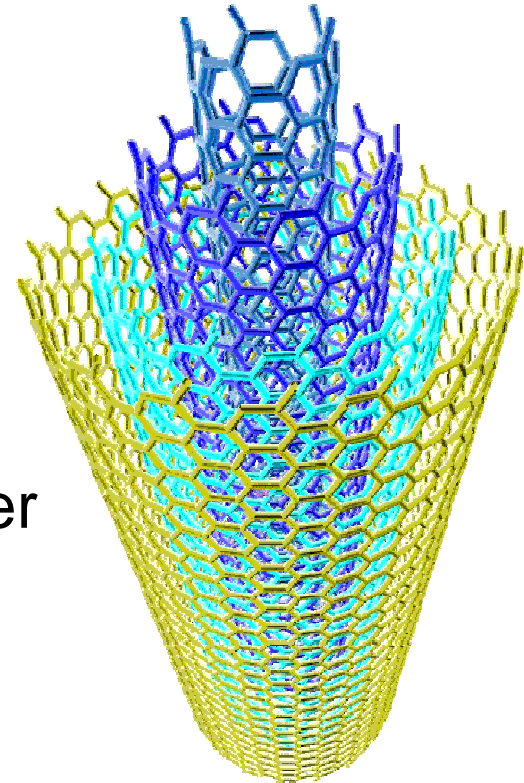
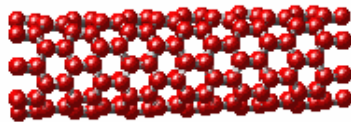


**300 mm Production Facility  
AMD Dresden (Germany)**



# Nanotech to the Rescue?

- Carbon nanotubes
  - Transistors
  - Storage
  - Wires
- Perhaps, but there's an even bigger picture . . .

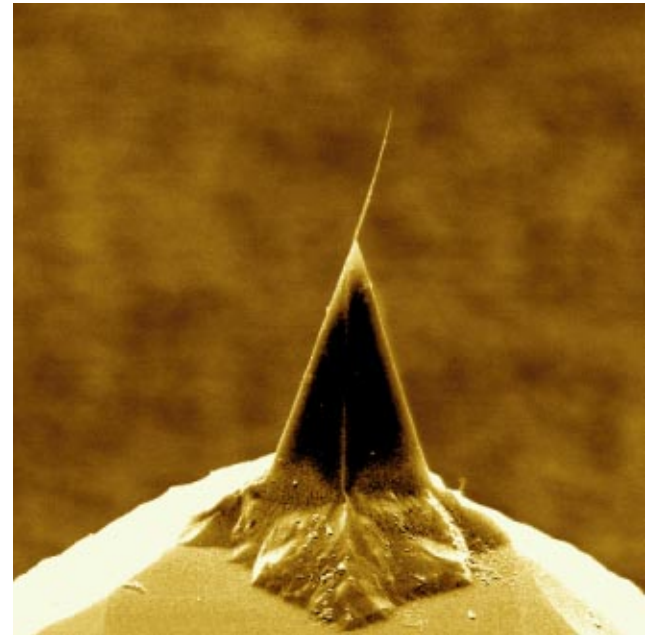


Carbon nanotube discovered  
by NEC corporate research  
center



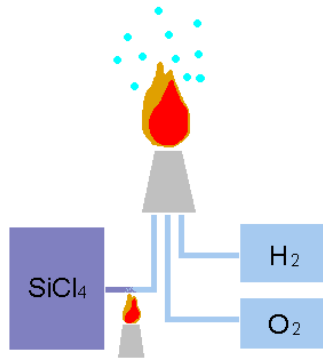
# Nanotech Applications

- Laboratory equipment for nanotech research
  - Microscopes
  - Instruments
- Bulk materials
  - Stain-proof clothing
  - Durable materials and paints
- Simple components
  - AFM tips
  - Transistors
  - Storage elements
  - displays
- NanoMEMS / nanomachines
- Nano fluidics
  - Biomedical applications
- Self assembly- polymers



**AFM tip**

# Applications of Colloidal Silica



Stiffen concrete (Key Bank Tower, Cleveland, OH)



Hard floor topcoats

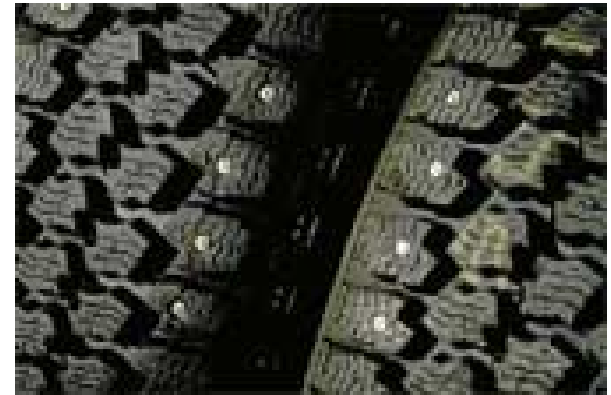
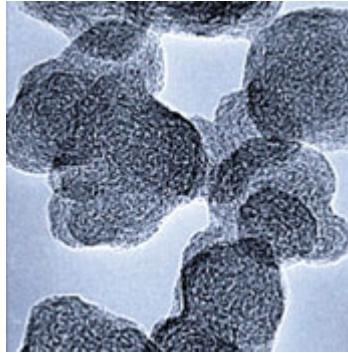


Chemical Mechanical Polishing (CMP)



High temperature transparent stove tops and semiconductor furnace tooling

# Carbon Black Additives



Tires



Paints and Inks



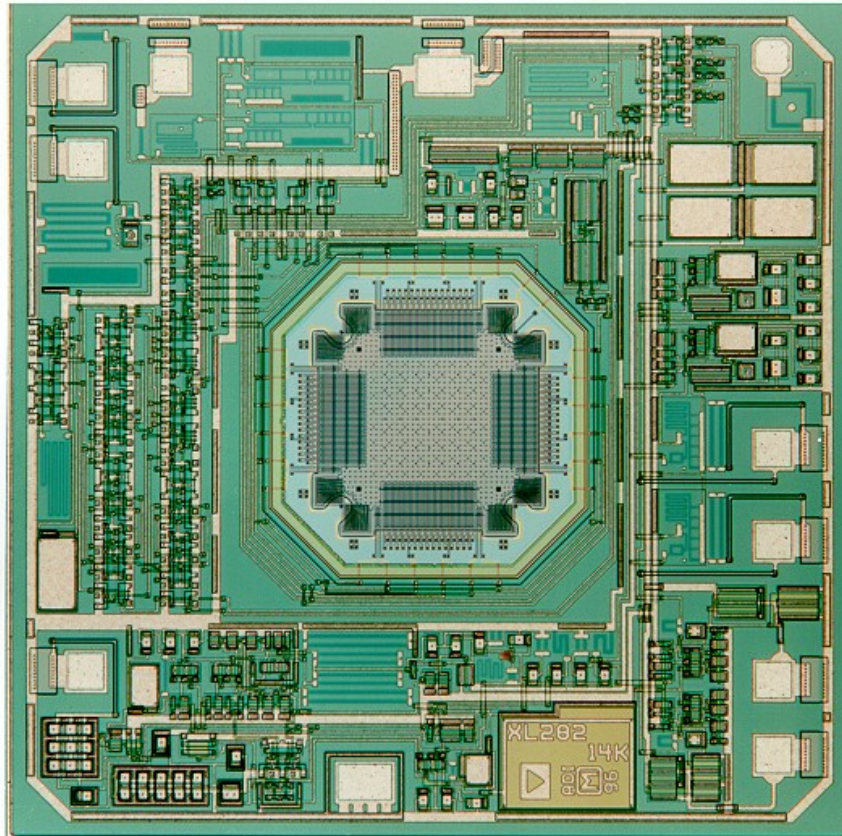
Car paints



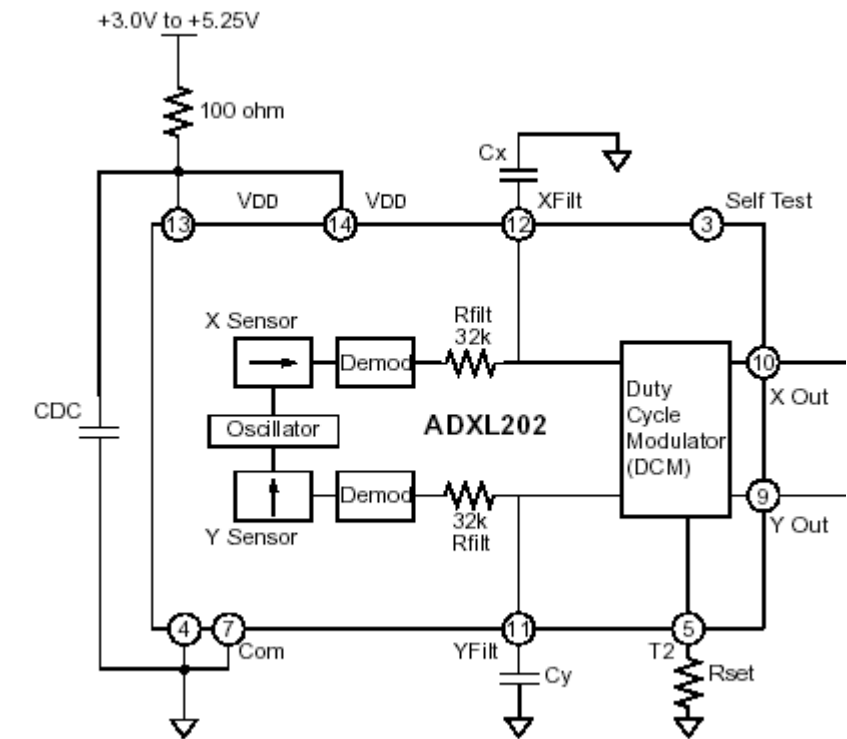
Conductive plastics



# Automotive MEMS: Accelerometer



ADXL202 BLOCK DIAGRAM



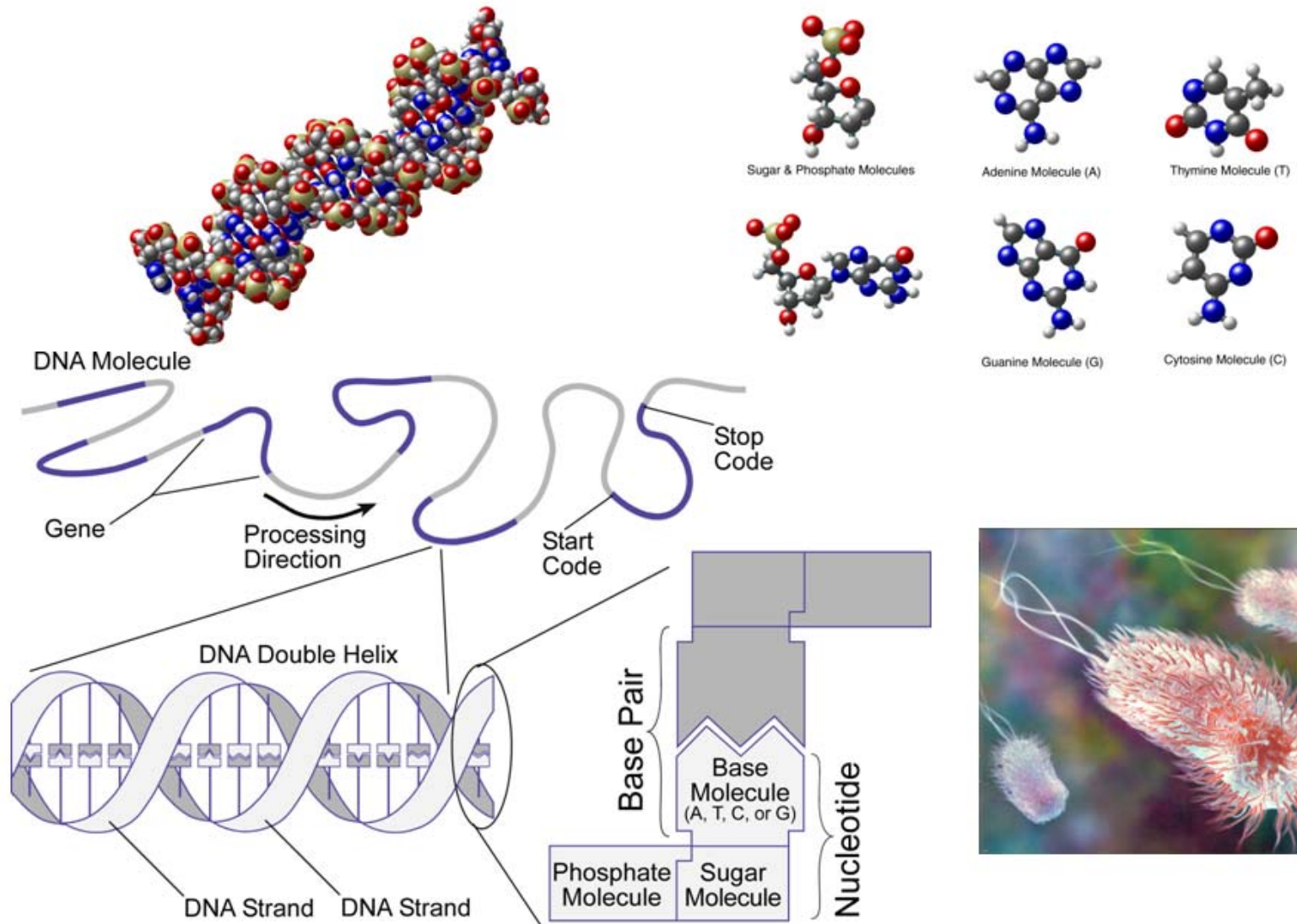
Analog Devices ADXL202

# Automotive MEMS: Tire Pressure

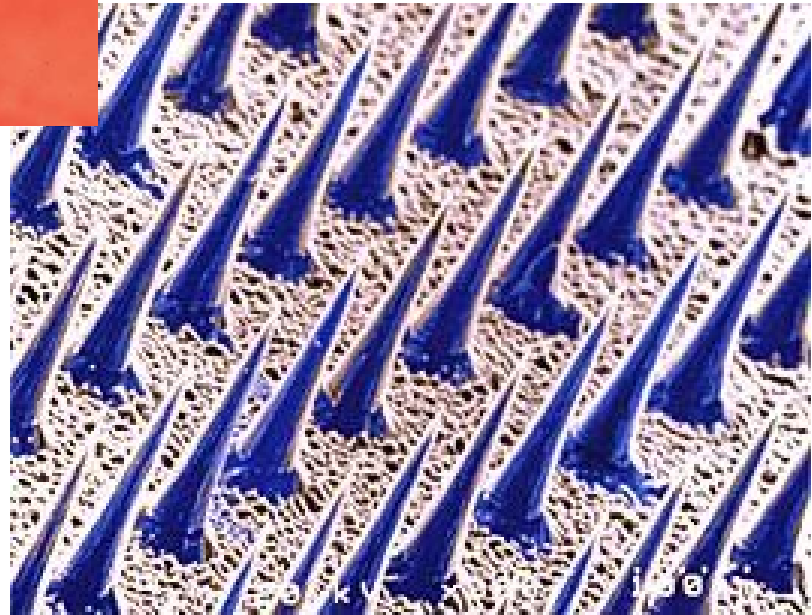
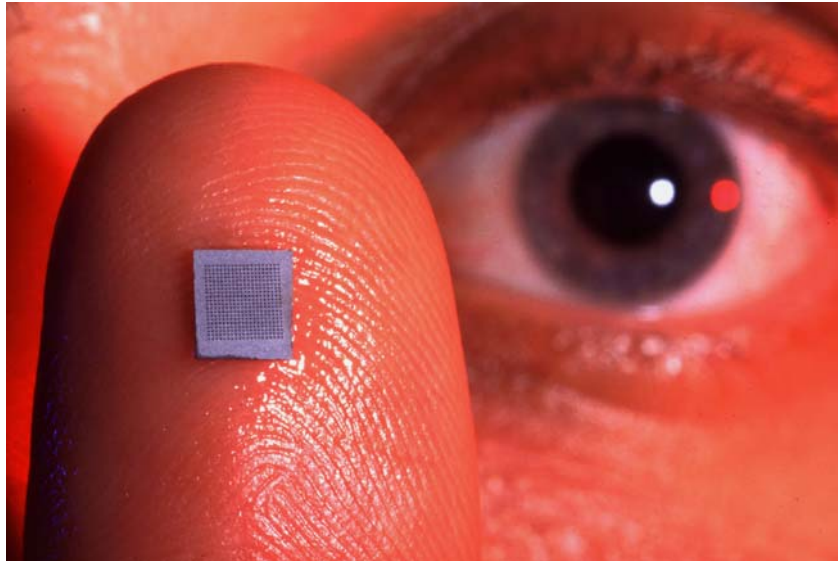




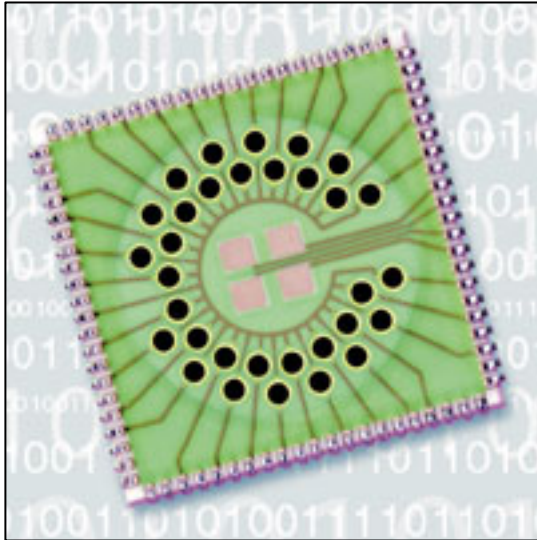
# Bioinformatics



# Biomedical MEMS: Microneedles

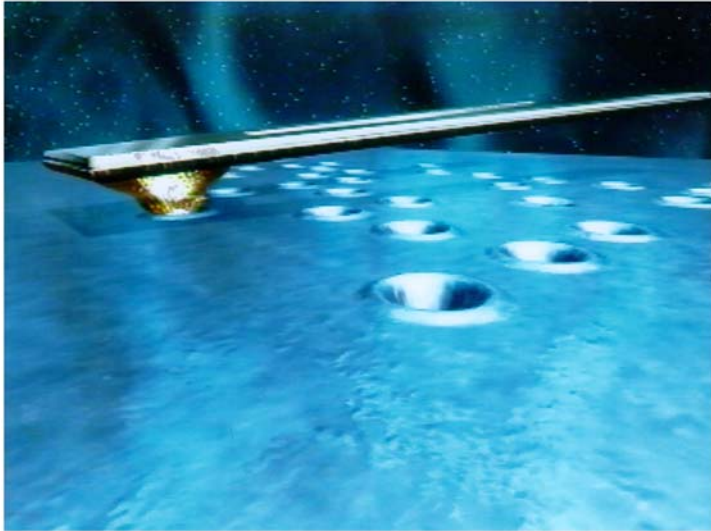


# Electronic Noses & Tongues



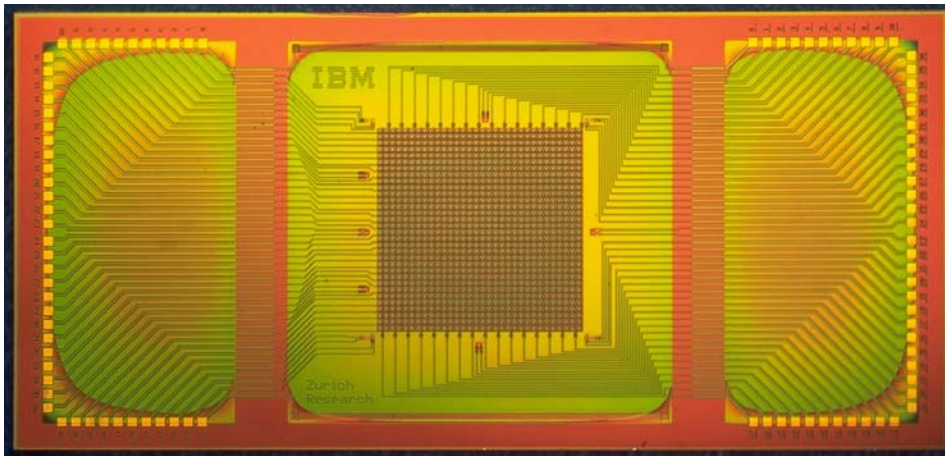
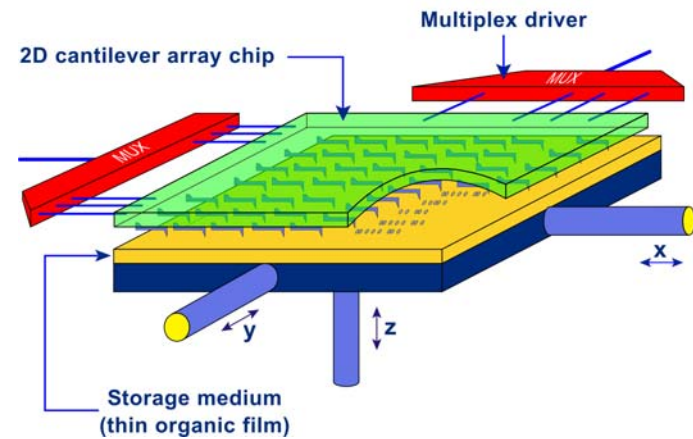


# Storage: IBM



## "MILLIPEDE"

Highly parallel, very dense AFM data storage system



# RFID: Texas Instruments

## Electronic Product Code (EPC)

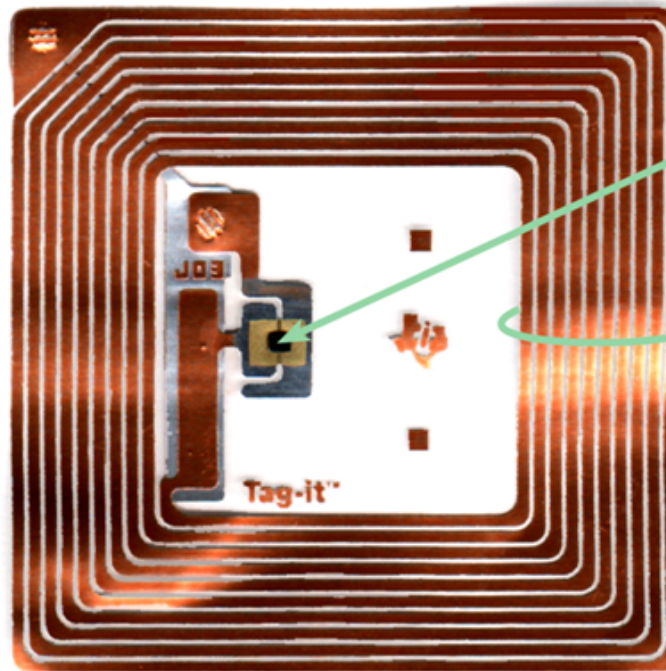
0A·3000FE4·00118BD·000999325

Header (8 bits)  
Type of code

EPC Manager (28 bits)  
Manufacturer of the product

Object class (24 bits)  
Like UPC's item number  
(describes item)

Serial number of  
item (36 bits)



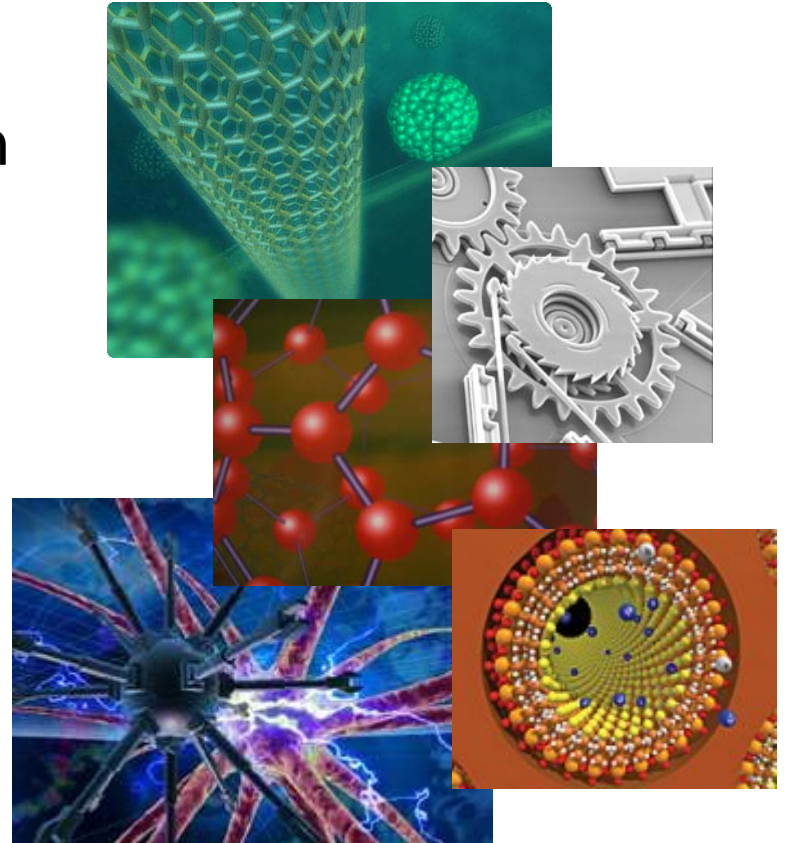
RFID chip

Antenna



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# The Economics Of Nanometer Design

## *65nm Technology, 300mm Wafers*

Process Technology R&D	~500 M\$/Year
------------------------	---------------

Pilot Line	1-2 B\$
------------	---------

Wafer Fab	3 B\$
-----------	-------

Design	15-30 M\$
--------	-----------

Masks' Set (35-40 Masks)	~3 M\$
--------------------------	--------

Test (SOC)	~15 ¢/Second
------------	--------------

# The Economics Of Nanometer Design

**45nm** Technology, 300mm Wafers

Process Technology R&D	~ <b>800</b> M\$/Year
------------------------	-----------------------

Pilot Line	1-2 B\$
------------	---------

Wafer Fab	3 B\$
-----------	-------

Design	<b>20-50</b> M\$
--------	------------------

Masks' Set (35-40 Masks)	<b>Up to 9</b> M\$
--------------------------	--------------------

Test (SOC)	constant
------------	----------

# Nanometer Design

*The Challenges Are Increasing*

188MT  
3.4GHz  
85-95W



**Uncertainty  
Variability**

125MT  
3.4GHz  
90-105W



**Leakage  
Lithography**

55MT  
2.2GHz  
55-95W



**SI  
CMP**

42MT  
1.4GHz  
55-75W



**Timing Closure  
Vias**

7.5MT  
300MHz  
35-45W



**Timing, Area  
Particles**

250 nm

180 nm

130 nm

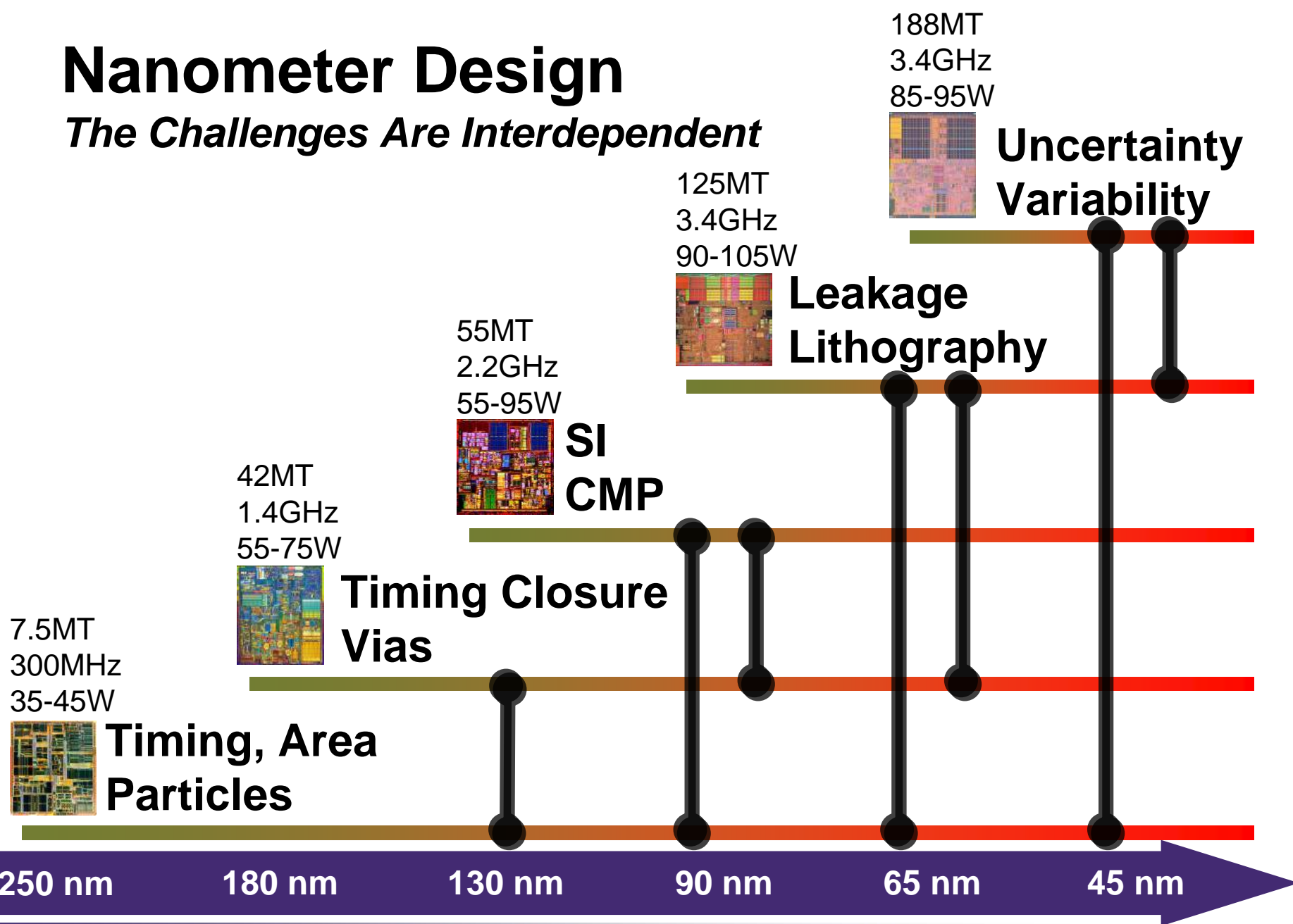
90 nm

65 nm

45 nm

# Nanometer Design

*The Challenges Are Interdependent*

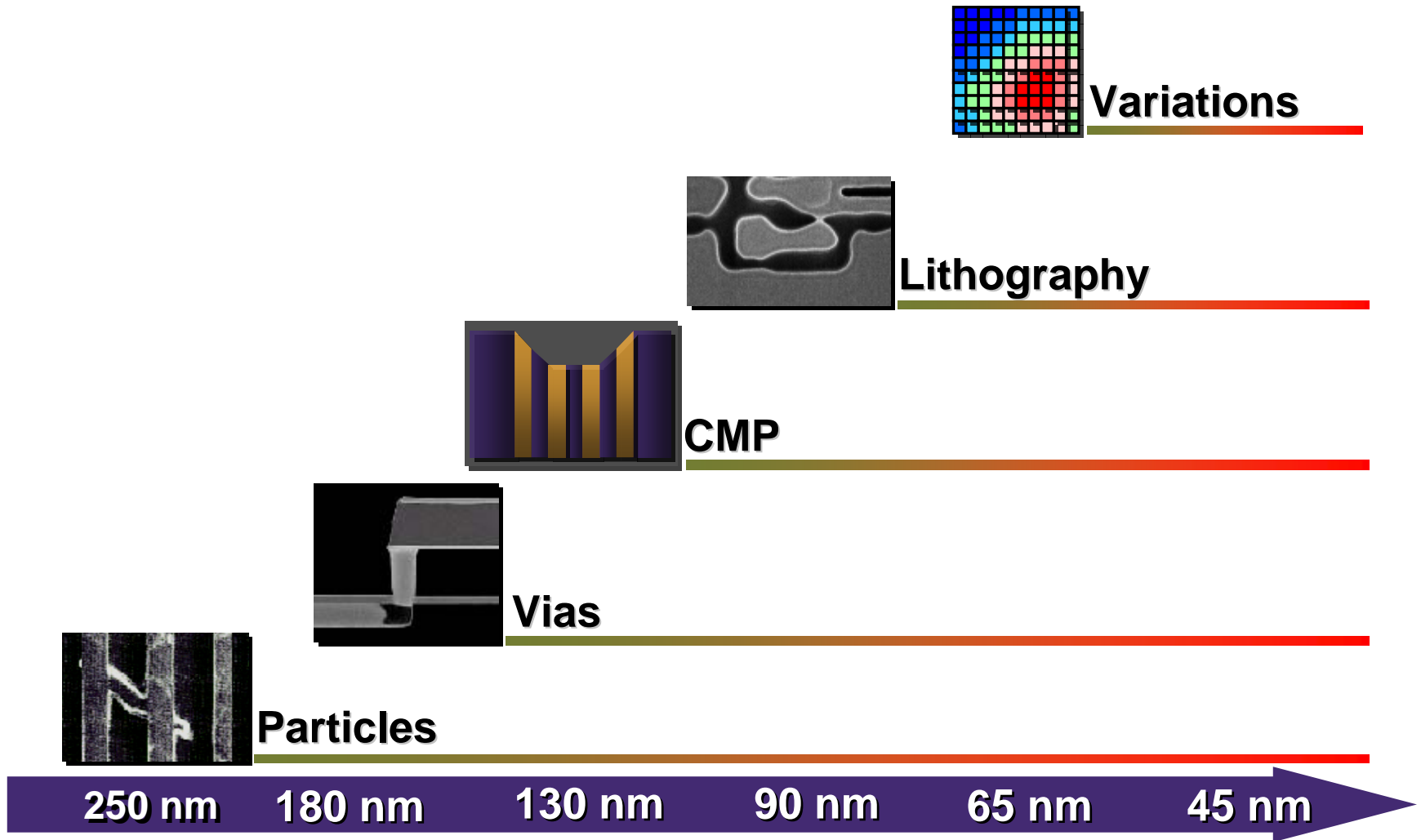




# Yield – What is it?

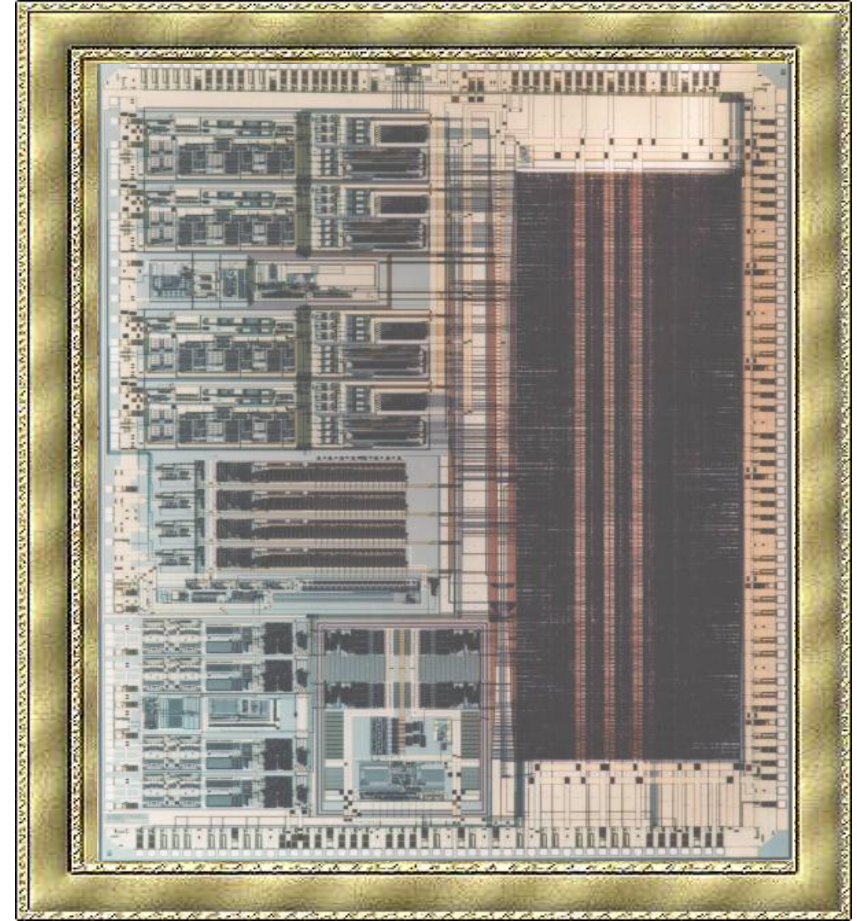
- Number of good chips / total chips
- Example – 64 chips test good (can be sold) out of a total number of 100 chips on the wafer, the yield would be 64% or 64/100.
- Reasons chip yield is not 100%
  - Defects originate in the design (line spacing is too close making the lines more susceptible to bridging by contamination)
  - Defects originate in the manufacturing process (imaging of a given pattern is not resolved causing the feature to not appear)
- DFM (Design for Manufacturing) software tools and solutions
  - Minimize design defects by considering how and under what conditions the design will be manufactured
  - Minimize manufacturing defects by providing a design robust enough to be manufactured within the given process.
- Designs that can't be manufactured (or manufactured at a profit) are just art work

# Yield Challenges Are Increasing

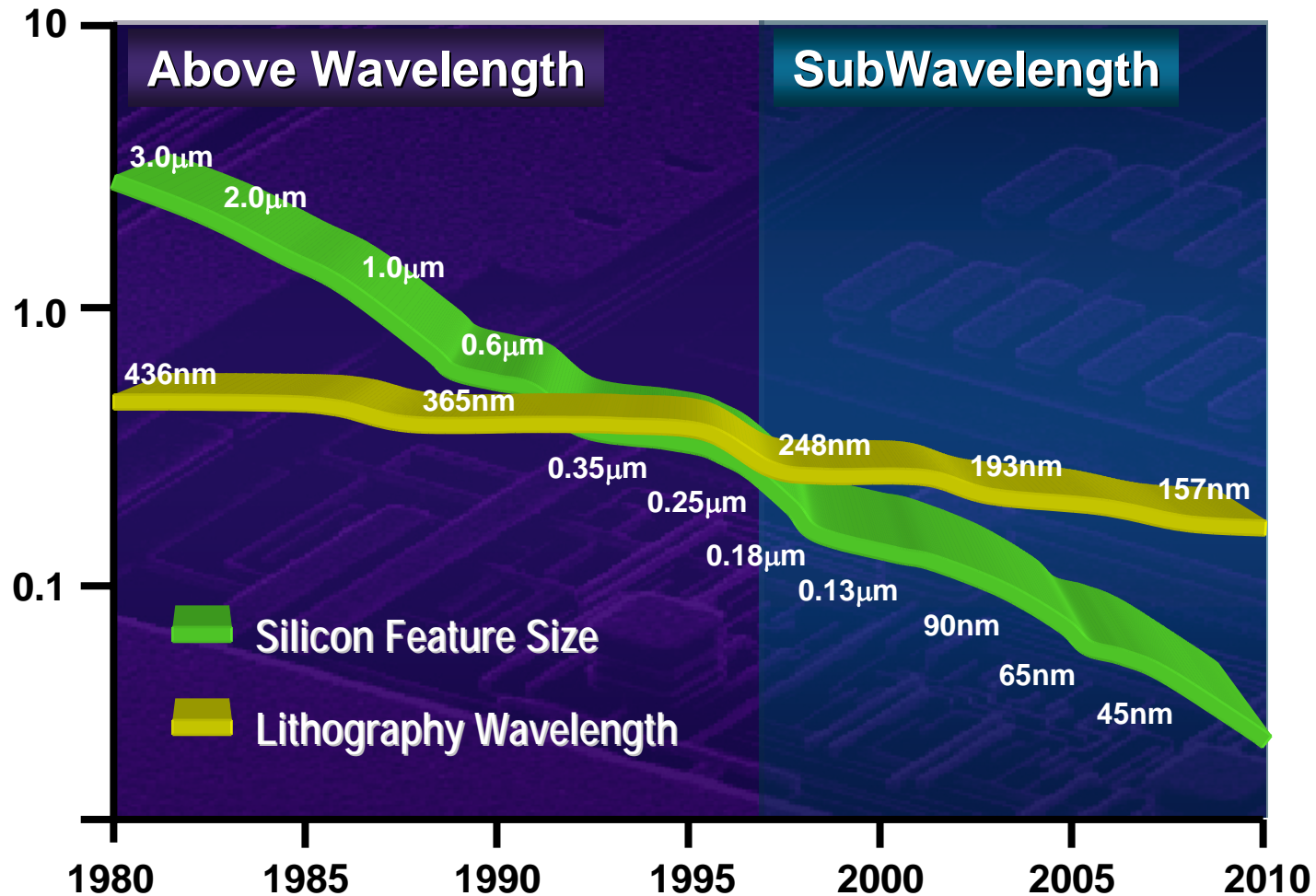


# Designs without Manufacturing...

...are just artwork



# Subwavelength Lithography Challenge



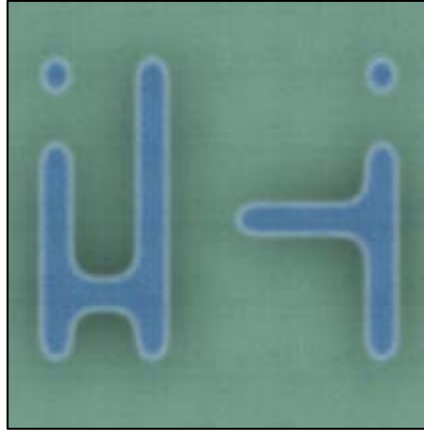


# What Does This Mean?

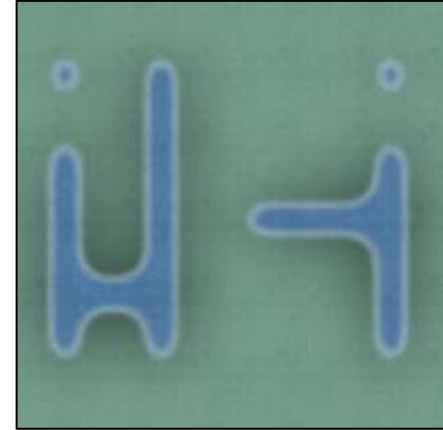
Layout



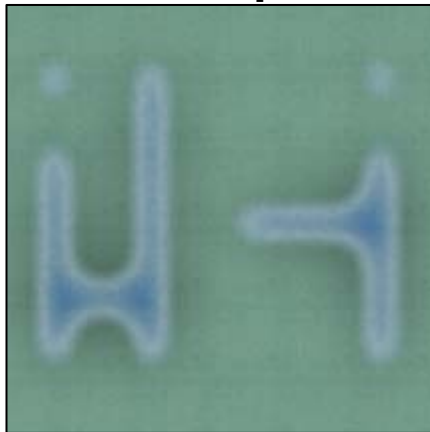
0.25 $\mu$



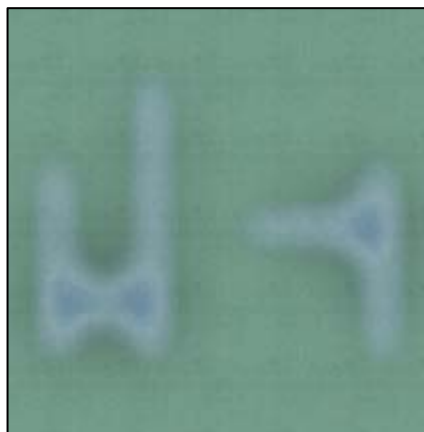
0.18 $\mu$



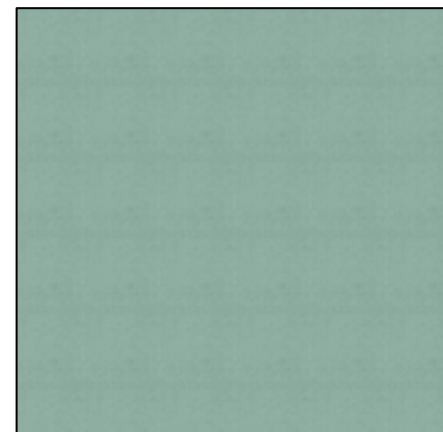
0.15 $\mu$



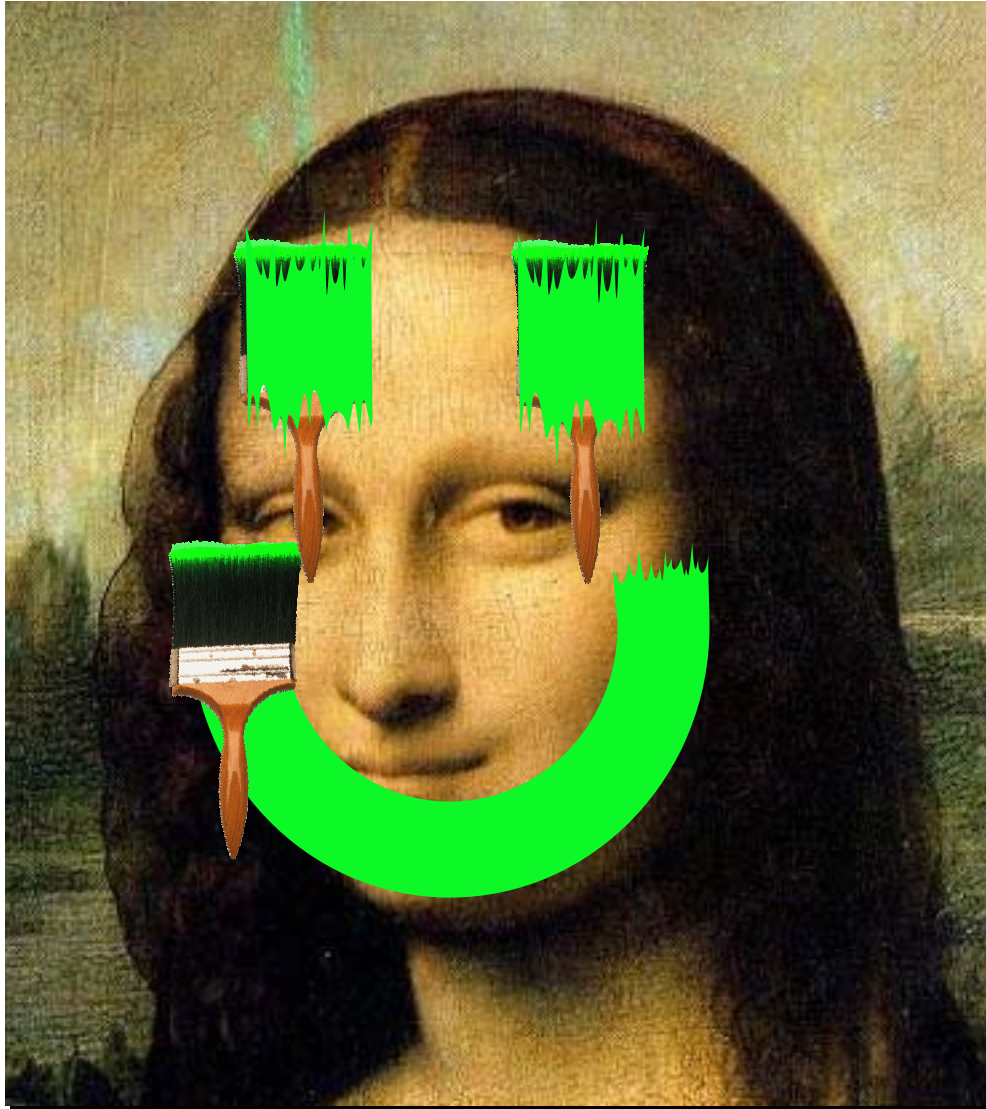
130nm



90nm

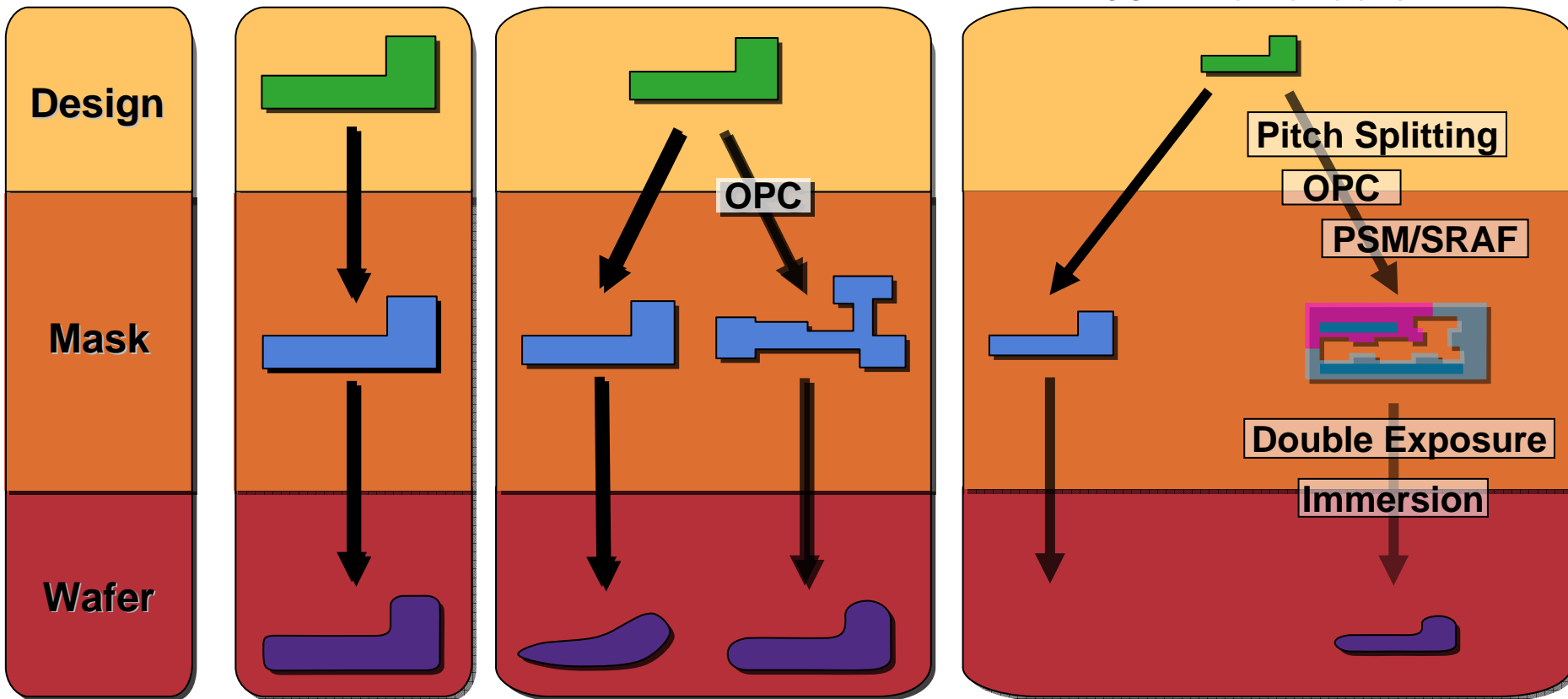


# DaVinci's House Paint Brush



# Sub-Wavelength Lithography Requires RET

193nm stepper



# What's Next in EDA?

- 1-2 Years

- System/Transaction Level C/C++ Design
- Asynchronous Design
- More Timing/Power/Yield Analysis and Optimization
- More Statistical Approaches to Computer Aided Design (CAD)
- More Design for Manufacturing (DFM)/Physical Design Interaction

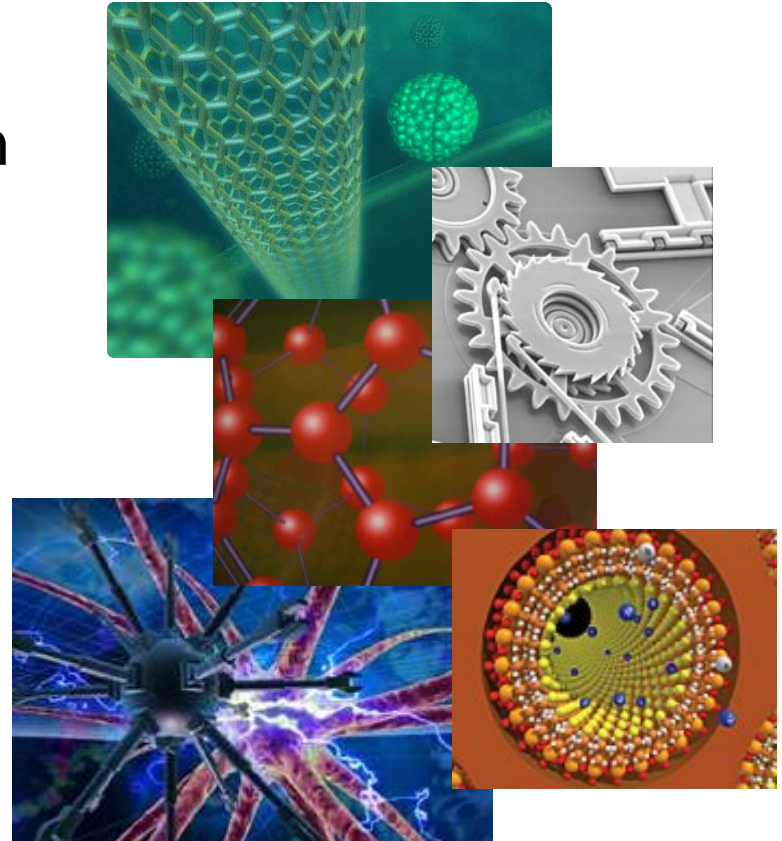
- 3-5 years

- Hardware/Software Design and Verification
  - Embedded Software Verification
- Error-Correcting Codes
- Micro-fluidics/Nano-fluidics
- MEMS/NEMS (Micro/Nano-Electro-Mechanical Systems)
- Nano-Technology
- Quantum Physical Effects



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# Summary

- The information revolution is beginning
  - Intelligent systems displace electromechanical systems
  - Intelligent systems interface with the real world, humans move to a supervisory role
- The transformation of entire industries is an electronics-based revolution
  - Nanotechnology complements and aids electronic systems in components and in sensors and actuators
  - Bioinformatics complements and aids electronic systems
- Nanotechnology is:
  - Enabled by progress in semiconductor electronics
  - Derived from progress in semiconductor electronics
  - Natural extension to semiconductor electronics

