High Performance and Low Power Programmable Bit Serial Digital down Converter Design Based on Half Band FIR Decimation

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Abstract—This paper proposes a novel Digital Down Converter (DDC) architecture for bit serial data, that can be used in digital receivers. The major advantage of proposed DDC is that the data is bit serial which results in reduced area and better timings. The proposed architecture is best suited for bit serial communication system with bit serial Analog to Digital Converter (ADC).

Key Words: digital down converter, digital receiver, multirate signal processing, polyphase decimation.

1. Introduction

Digital down-converters (DDCs) have wide applications in digital receivers in wireless communications systems. The major advantages of DDC include the increased stability over temperature and time and complete elimination of some impairment due to analogue circuits (e.g., mismatches between analog I and Q channels). Off-the-shelf DDCs are now Commercially available from Analog Device, TEXAS INSTRUMENTS, and other manufactures. All these products, however, use Cascaded Integrator-Comb (CIC) filters **for** large decimation to reduce complexity and power consumption [I] as shown in fig.1. The principle goal of the DDC is to filter and translate a desired band to baseband. The decimation occurs in two steps process. The center of the band of interest is shifted to DC by the quadrature modulator, the real and imaginary outputs are each passed to a High Decimation Filter (HDF) as shown in fig.2. The outputs of the HDF filters must be scaled for gain compensation. The lowpass response of the HDF has a gradual roll off characteristic requiring a subsequent conventional FIR to achieve a sharp transition. The DDC employs a fixed shaping filter for ease of use. The output bandwidth of the DDC is a function of the input sampling rate, the HDF decimation factor and the fixed shape of the FIR which in return decimates as much as desired.

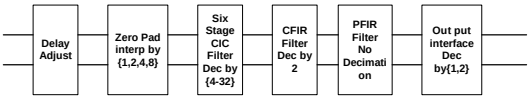

fig. 1 Digital Down converter Filtering Block Diagram

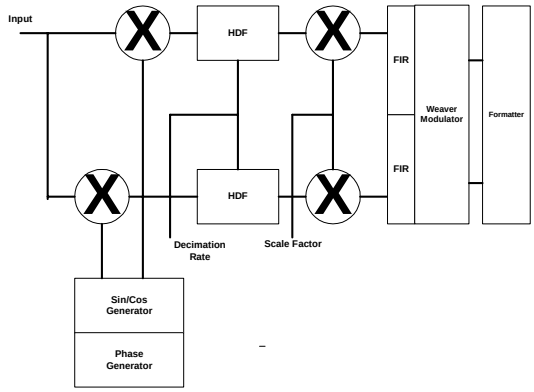

fig. 2 Basic Digital Down converter Block Diagram

The FIR filter's passband compensates for the roll off inherent in the passband of the HDF filter to meet the goal of a low passband ripple [1].

2. Digital Down Converter Filtering

The Digital down converter filtering block diagram is shown in fig.1. Cascaded integrator-comb (CIC), or Hogenauer filters, are multirate filters used for realizing large sample rate changes in digital systems[2]. CIC filters are multiplierless structures, consisting of only

adders, subtractors and registers. They are typically employed in applications with large excess sample rate i.e, the system sample rate is much larger than the bandwidth occupied by the signal.
A coarse gain adjustment may be applied at the output of the CIC filter to compensate for the bandwidth reduction performed by the CIC decimator. The signal stream from the CIC can be filtered by two additional stages of filtering. The *compensation finite impulse response (CFIR)* filter and the *programmable finite impulse response (PFIR)* filter. These are optional stages of processing that may be inserted or excluded from the datapath. The CFIR and PFIR can be single rate or polyphase multirate filter structures.

3.Bit Serial Programmable Digital Down Converter

From the general block diagram of Digital down converter fig.1 and fig.2 we see that it is basically a stage wise decimation and the decimation factor is based on the input data rate and the required output rate, in order to make our DDC bit serial we first need to make bit serial polyphase decimation FIR filter which is the basic building block of DDC[3], and after that by cascading different polyphase FIR stages we can make our DDC work.

3.1 Formulation of Bit Serial Parallel FIR Using Polyphase Decimation

The polyphase decimator is a polyphase filter with an embedded 2-to-1 down sampling of input signal, the structure as shown in fig .3.
The polyphase segments are accessed by delivering the input samples $x(n)$ to their inputs via an input commutator which starts at the segment index and decrements to index 0. After the commutator as executed one cycle and delivered M input samples to the filter, a single output is taken as the summation of the outputs from the polyphase segments. The output sample rate is half the sample rate of the input data stream.
An N-tap FIR filter can be expressed in time domain as

$$y(n)=h(n)*x(n)=\sum_{i=0}^{N-1}h(i)x(n-i), \quad n=0,1,2,...\infty \tag{3.1}$$

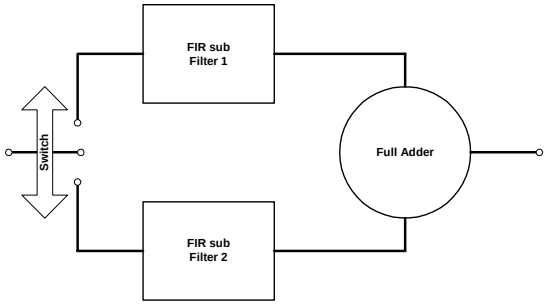

fig. 3 Polyphase Half Band Decimator

Where {x(n)} is an infinite length input sequence and {h(n)} contains FIR coefficients of length N, or in Z-domain as

$$Y(z)=H(z)X(z)$$
$$=\sum_{n=0}^{N-1}h(n)z^{-n}\sum_{n=0}^{\infty}x(n)z^{-n} \tag{3.2}$$

The input sequence {x(0),x(1),x(2),…}can be decomposed into even numbered part and odd numbered part as follows:

$$X(z)=x(0)+x(1)z^{-1}+x(2)z^{-2}+x(3)z^{-3}+...$$
$$=x(0)+x(2)z^{-2}+x(4)z^{-4}+...$$
$$+z^{-1}[x(1)+x(3)z^{-2}+x(5)z^{-4}+.....] \tag{3.3}$$
$$=X_0(z^2)+X_1(z^2)$$

Where $X_0(z^2)$ and $X_1(z^2)$ are the Z- transforms of x(2k) and (2K+1).
Similarly the Length-N filter coefficients H(Z) can be decomposed as

$$H(z)=H_0(z^2)+H_1(z^2) \tag{3.4}$$

where $H_0(z^2)$ and $H_1(z^2)$ are of length N/2 and are referred as even sub filter and odd sub filter

$$Y(z)=Y_0(z^2)+z^{-1}Y_1(z^2)$$
$$=(X_0(z^2)+z^{-1}X_1(z^2))(H_0(z^2)+z^{-1}H_1(z^2))$$
$$=X_0(z^2)H_0(z^2)+z^{-1}(X_0(z^2)H_1(z^2)$$
$$+X_1(z^2)H_0(z^2))+z^{-2}(X_1(z^2)H_1(z^2) \tag{3.5}$$

i.e

$$Y_0(z^2)=X_0(z^2)H_0(z^2)+z^{-2}(X_1(z^2)H_1(z^2) \quad (3.6)$$

$$Y_1(z^2)=X_0(z^2)H_1(z^2)+X_1(z^2)H_0(z^2)$$

where $Y_0(z^2)$ and $Y_1(z^2)$ corresponds to y(2k) and y(y2k+1) in time domain .the filtering operation processes two inputs x(2k) and x(2k+1) and generates two outputs y(2k) and y(2k+1) every iteration and this is poly phase decomposition

3.2 Design Example of Bit Serial FIR Sub Filter

The 4 tap FIR filter as an example is discussed for easy understanding, the equation is as follows :

$$Y(n) = -(7/8)x(n) - (7/8)x(n-1) + (1/2)x(n-2) + (1/2)x(n-3) \quad (5.1)$$

The signal word length is w, the above equation can be rewritten as follows

$$Y(n) = -x(n) + x(n)2^{-3} + x(n-1)2^{-1} \quad (5.2)$$

world level signal flow graph of the shift add
The sub filters are as follows

$$Y1(n) = (-7/8)x(n) + (1/2)x(n-1) \quad (5.3)$$

$$Y2(n) = (-7/8)x(n) + (1/2)x(n-1) \quad (5.4)$$

The signal word length of both the sub filters is w/2.

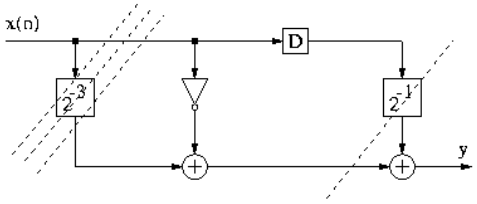

fig. 4 FIR Sub Filter with scaling operator

The word level signal flow graph of the shift –add based FIR filter is shown in fig.4. Due to presence of non causal scaling operators the design can be made feasible be adding Pipelining cut sets to it and there by delaying the advance scaling operator [4]. By placing delay elements along the cutsets and replacing the delayed scaling operators with switches, a feasible bit –level pipelined bit-serial FIR filter is derived as shown in fig.5. Here the word-level delay is equivalent to W bit level delays for a signal of word length of W.

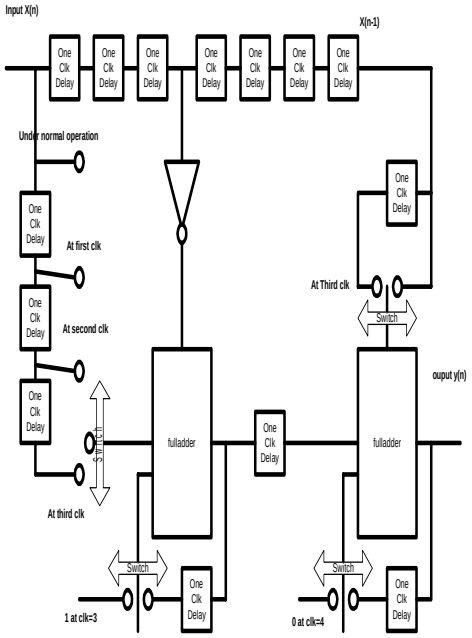

fig. 5 Bit Level Pipelined FIR Sub Filter

3.3.Polyphase bit Serial FIR decimator with decimation factor 2

Bit serial FIR decimator is a polyphase filter with an embedded 2-to-1 down sampling of input signal, Each polyphase segment is operating at a low output sample rate as compared to high input sample rate and total of N operations are performed per output point. Input is bit serial and it is given to both the sub filters after passing through a switch, switching at the data rate .the sub filters are operating at half the data rate, finally the output of both the filters is added and for a signal word length of w, w/2 alternate bits are given to each subfilter by the switch and at the end we get signal of word length w/2.
The basic 2-to-1down converter is shown in fig. 6

3.4. Simulation Synthesis and Implementation of Polyphase decimator

To Verify the correctness of the programmable polyphase half band decimator for Digital down converter, simulation is performed using Modelsim and Matlab the results were compared and then the hardware was developed using Xilinx FPGA[5][6].
For an input sequence of 11111111 binary with filter coefficient -7/8, -7/8, 0.5, 0.5 the output of polyphase decimator is shown in fig.8,Note that the out put 0100 occurs in bit serial manner .For

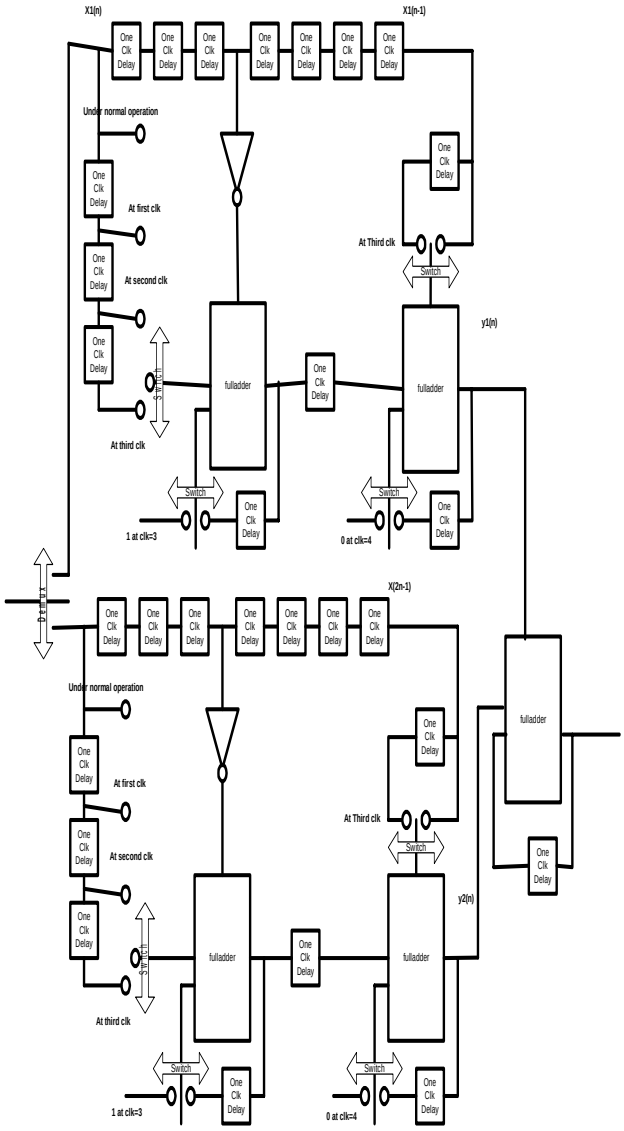

fig. 6 Basic 2-to-1 Polyphase Decimator

each out put the LSB occurs first and then the next LSB follows and so on. Same result is achieved using non polyphase decimation shown in fig.10. After the functionality is investigated in Verilog, the polyphase decimator and simple decimator are synthesized to schematic using Xilinx tool and the schematics are shown in fig.7 and fig.8 respectively.

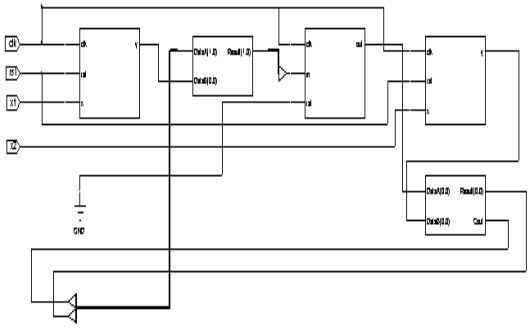

fig 7.0 Schematic for Bit level polyphase decimator

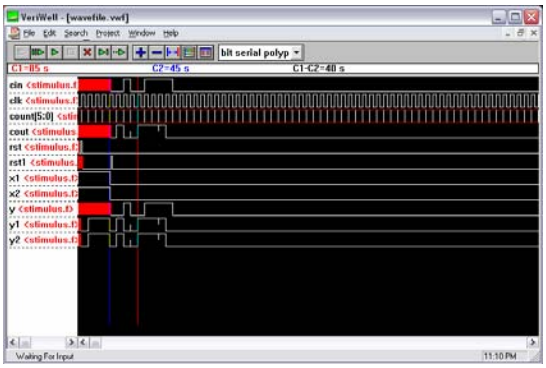

fig 8.0 Simulation wave form for bit level polyphase decimation

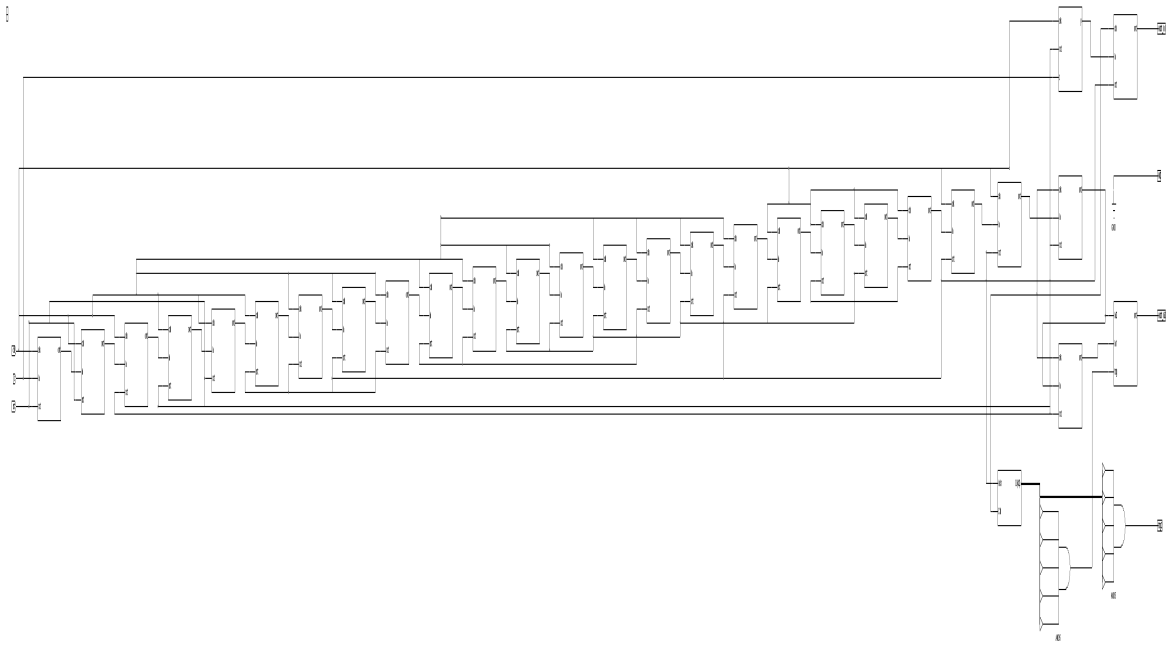

fig 9.0 Schematic for Bit level decimator

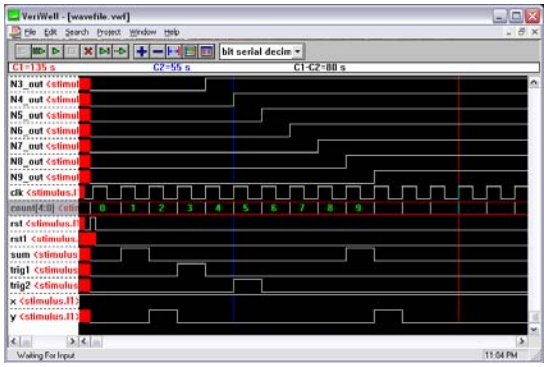

fig.10 Simulation wave form for bit level decimation

8.CONCLUSION

In this paper, we designed a programmable bit serial digital down converter using bit serial polyphase decimation technique. The key functional block of bit serial digital down converter i.e bit serial polyphase decimator has been implemented in detail, by cascading different such filters the full bit serial down converter can be realized. The bit serial polyphase decimator is very compact area wise and clock cycle is also shortened by using the bit serial FIR sub filters.

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