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VLSI DESIGN AND IMPLEMENTATION OF SYSTOLIC TREE QUEUES
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Abstract

A number of innovative designs have been proposed for hardware implementation of data structures. However, these designs have only been presented at an abstract behavioural level. In this paper, we describe the VLSI design and implementation of a 15-node 8-bit queue based on a systolic tree architecture. A layout methodology and a VLSI CAD environment that facilitate fast and efficient layout of large binary trees are described. The objective of this paper is to illustrate the implementation of tree architectures in VLSI. We demonstrate this by implementing a systolic tree queue.

Keywords: VLSI design; systolic tree architecture; automated layout