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BIT-SLICE MICROPROCESSOR-BASED COMMUNICATIONS DECODER
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Abstract

The hardware design of a bit-slice microprocessor-based realtime cyclic error-correcting communications decoder is presented. A microprocessor-based architecture is preferred because of its programmability, low cost and simplicity of design. To augment the throughput of the decoder for realtime decoding, the ALU word length is chosen to be equal to that of a code word and the decoding operation is accomplished in two steps, i.e. error detection and error correction. A buffer memory stores incoming blocks as more than one block may be received during a decoding cycle. The design is versatile: different decoding algorithms can be executed by changing the microprogram. Only simple changes in the design are necessary to decode words of longer block length.

Keywords: microprocessors; digital communications; decoding