COE 301/ICS 233 – Computer Organization

Term 212 – Spring 2022

Project: Pipelined Processor Design

Objectives:

- Designing a Pipelined 32-bit RISC processor with 32-bit instructions
- Using the Logisim simulator to model and test the processor
- Teamwork

Instruction Set Architecture

In this project, you will design a RISC processor that has 31 general-purpose 32-bit registers: R1 to R31. Register R0 is hardwired to zero. Reading R0 always returns the value 0. Writing R0 has no effect. The value written to R0 is discarded.

All instructions are 32-bit long and aligned in memory. Memory is word (32-bit) addressable. The PC register (20-bit wide) contains the instruction address. There are three instruction formats: R-type, I-type, and SB-type as shown below:

R-type

6-bit opcode (Op), 5-bit register numbers (*rs1*, *rs2*, and *rd*), and 11-bit function field (*f*)

f^{11}		$rs2^5$		$rs1^5$		rd^5		Op^6	
31	21	20	16	15	11	10	6	5	0

I-type

6-bit opcode (Op), 5-bit register numbers (*rs1* and *rd*) and 16-bit Immediate

imm16		$rs1^5$		rd^5		Op^6	
31	16	15	11	10	6	5	0

SB-type

6-bit opcode (Op), 5-bit register numbers (*rs1* and *rs2*) and 16-bit Immediate split into (imm11U and imm5L)

imm11U		$rs2^5$		$rs1^5$		imm5L		Op^6	
31	21	20	16	15	11	10	6	5	0

Rs1 is the first source register number. This register is always read (never written). Ra is the name and value of register rs1.
Rs2 is the second source register number. This register is always read (never written). Rb is the name and value of register rs2.
Rd is the destination register number. This register is always written (never read). Rd is the name and value of destination register rd.

Instruction Encoding

The R-type, I-type, and SB-type instructions, meanings, and encodings are shown below:

Instruction	Meaning	Encoding				
SLL	Rd=ShiftLeftLogical(Ra, Rb[4:0])	f=0	rs2	rs1	rd	Op=0
SRL	Rd=ShiftRightLogical(Ra, Rb[4:0])	f=1	rs2	rs1	rd	Op=0
SRA	Rd=ShiftRightArith(Ra, Rb[4:0])	f=2	rs2	rs1	rd	Op=0
ROR	Rd=RotateRight(Ra, Rb[4:0])	f=3	rs2	rs1	rd	Op=0
ADD	Rd=Ra + Rb	f=4	rs2	rs1	rd	Op=0
SUB	Rd=Ra – Rb	f=5	rs2	rs1	rd	Op=0
SLT	Rd=(Ra < Rb) signed	f=6	rs2	rs1	rd	Op=0
SLTU	Rd=(Ra < Rb) unsigned	f=7	rs2	rs1	rd	Op=0
XOR	Rd=Ra ^ Rb	f=8	rs2	rs1	rd	Op=0
OR	Rd=Ra | Rb	f=9	rs2	rs1	rd	Op=0
AND	Rd=Ra & Rb	f=10	rs2	rs1	rd	Op=0
NOR	Rd = ~(Ra | Rb)	f=11	rs2	rs1	rd	Op=0
MUL	Rd = (Ra * Rb)[31:00]	f=12	rs2	rs1	rd	Op=0
SLLI	Rd=ShiftLeftLogical(Ra, sa)	0	sa	rs1	rd	Op=1
SRLI	Rd=ShiftRightLogical(Ra, sa)	0	sa	rs1	rd	Op=2
SRAI	Rd=ShiftRightArith(Ra, sa)	0	sa	rs1	rd	Op=3
RORI	Rd=RotateRight(Ra, sa)	0	sa	rs1	rd	Op=4
ADDI	Rd=Ra + sign_extend(imm16)	imm16		rs1	rd	Op=5
SLTI	Rd=(Ra < sign_extend(imm16)) signed	imm16		rs1	rd	Op=6
SLTIU	Rd=(Ra < sign_extend(imm16)) unsigned	imm16		rs1	rd	Op=7
XORI	Rd=Ra ^ zero_extend(imm16)	imm16		rs1	rd	Op=8
ORI	Rd=Ra | zero_extend(imm16)	imm16		rs1	rd	Op=9
ANDI	Rd=Ra & zero_extend(imm16)	imm16		rs1	rd	Op=10
NORI	Rd = ~(Ra | zero_extend(imm16))	imm16		rs1	rd	Op=11
LUI	Rd=imm16<<16	imm16		0	rd	Op=12
JALR	PC=Ra+sign_extend(imm16), Rd=PC+1	imm16		rs1	rd	Op=13
LW	Rd=Mem[Ra+sign_extend(imm16)]	imm16		rs1	rd	Op=14
SW	Mem[Ra+sign_extend({imm11U, imm5L})]=Rb	imm11U	rs2	rs1	imm5L	Op=15
BEQ	if (Ra == Rb) PC=PC+sign_extend({imm11U, imm5L})	imm11U	rs2	rs1	imm5L	Op=16
BNE	if (Ra != Rb) PC=PC+sign_extend({imm11U, imm5L})	imm11U	rs2	rs1	imm5L	Op=17
BLT	if (Ra < Rb) PC=PC+sign_extend({imm11U, imm5L})	imm11U	rs2	rs1	imm5L	Op=18
BGE	if (Ra >= Rb) PC=PC+sign_extend({imm11U, imm5L})	imm11U	rs2	rs1	imm5L	Op=19
BLTU	if (Ra < Rb) unsigned PC=PC+sign_extend({imm11U, imm5L})	imm11U	rs2	rs1	imm5L	Op=20
BGEU	if (Ra >= Rb) unsigned PC=PC+sign_extend({imm11U, imm5L})	imm11U	rs2	rs1	imm5L	Op=21

Instruction Description

Opcodes 0 is used for R-format ALU instructions. There are 13 instructions in total.

Opcodes 1 through 14 are used for I-format instructions. There are 14 instructions in total.

The I-format ALU instructions (**SLLI** through **NORI**) have identical functionality as their corresponding R-format instructions (**SLL** through **NOR**), except that the second ALU operand is an immediate constant. The **imm16** immediate value is sign extended for all instructions except bitwise logical instructions (**XORI**, **ORI**, **ANDI**, and **NORI**) where the constant is zero extended.

Opcode 14 define load word (**LW**) instruction. This instruction addresses 4-byte words in memory. The effective memory address = **Ra + sign_extend(imm16)**.

Opcode 15 define store word (**SW**) instruction. This instruction addresses 4-byte words in memory. The effective memory address = **Ra + sign_extend({imm11U, imm5L})**..

There are six branch instructions **BEQ** to **BGEU** with opcodes 16 to 21 and PC-relative addressing. If the branch is taken, then **PC = PC + sign_extend({imm11U, imm5L})**. Otherwise, **PC = PC + 1**. The conditional branch range is **[-32768, +32677]**.

Opcode 12 define load upper immediate (**LUI**) instruction. **LUI** is used to build 32-bit constants and uses the I-type format. **LUI** places the **imm16** value in the upper 16 bits of the destination register ***Rd***, filling the lowest 16 bits with zeros.

Opcode 13 defines the **JALR** (Jump-And-Link-Register) instruction. It saves the return address in **Rd** (**Rd = PC+1**) and does an indirect register jump with an offset (**PC = Ra + sign_extend(imm16)**). If **Rd** is **R0** then the return address (**PC+1**) is not saved, and **JALR** becomes a Jump Register (**JR**) pseudo-instruction. If **Ra** is **R0**, then **JALR** instruction becomes a Jump and link (**JAL**) pseudo-instruction. If both **Ra** and **Rd** are **R0**, then **JALR** instruction becomes a Jump (**J**) pseudo-instruction. To use **JALR** instruction, follow the following syntax: **JALR RD, RS1, imm16**.

Memory

Your processor will have separate instruction and data memories. The PC register should be 20 bits. The instruction memory can store 2^{20} instructions, where each instruction occupies four bytes. There are 1048576 (1M) instructions in the instruction memory.

The data memory will also be to 2^{20} words = 4 Mi Bytes. The data memory is *word addressable*, since only the LW and SW instructions address memory. Words should be always aligned in memory. The ALU result represent the address for the data memory.

Addressing Modes

PC-relative addressing mode is used for branch and jump instructions.

For taken branches: PC = PC + sign_extend({imm11U, imm5L})

For JALR: PC = Ra + sign_extend(imm16)

For LW, displacement addressing is used: Memory address = Ra + sign_extend(imm16)

For SW, displacement addressing is used: Memory address = Ra+sign_extend ({imm11U, imm5L})

Register File

Implement a Register file containing 32 (thirty-two) 32-bit registers R0 to R31 with two read ports and one write port. R0 is a special register that can only be read not written (hardwired to zero).

Register Rs1 is always read by all instructions (never written).

Register Rs2 is always read by R-type and SB-type instructions.

Register Rd is written by R-type and I-type instructions.

Arithmetic and Logic Unit (ALU)

Implement a 32-bit ALU to perform all the required operations:

ADD, SUB, SLT, SLTU, XOR, OR, AND, NOR, SLL, SRL, SRA, ROR, MUL

In addition, you should have special support for the LUI instruction.

Program Execution

The program will be loaded and will start at address 0 in the instruction memory. The data segment will be loaded and will start also at address 0 in the data memory. You can also have a stack segment to support procedures. The stack segment can occupy the upper part of the data memory and can grow backwards towards lower memory addresses. The stack segment is implemented completely in software. You can dedicate register R30 as the stack pointer. To terminate the execution of a program, the last instruction in the program can jump to itself indefinitely.

Build a Single-Cycle Processor

Start by building the datapath and control of a single-cycle processor and ensure its correctness. You should have sufficient test cases that ensure the correct execution of ALL instructions in the instruction set. You should also write test cases that show the correct execution of complete programs. To verify the correctness of your design, show the values of all registers in the register file (R0 to R31) at the top-level of your design. Provide output pins for all registers R0 through R31 and make their values visible outside the register file.

Build a Pipelined Processor

Once you have succeeded in building a single-cycle processor and verified its correctness, design and implement a pipelined version of your design. Make a copy of your single-cycle design, then convert it and implement a pipelined datapath and its control logic. Add pipeline registers between stages. Design the control logic to detect data dependencies among instructions and implement the forwarding logic. You should handle properly the control hazards of the branch and jump instructions. Also, stall the pipeline after a LW instruction if it is followed by a dependent instruction.

Design Alternatives

When designing the datapath and control unit, explore alternative design options and justify why a given design alternative is chosen. For example, when designing the control unit consider implementing it using a decoder and a set of OR/NOR gates, versus using a ROM to store the control signals, versus optimizing the equation of each control signal separately. When designing

the ALU and the shifter unit, consider alternative designs and justify why a design alternative is chosen. The same should be applied for all design decisions in your CPU, such as handling control and data hazards in the pipeline.

Testing

To demonstrate that your CPU is working, you should do the following:

1. Write a sequence of instructions to verify the correctness of ALL instructions. Use LUI and ORI to initialize registers. Demonstrate the correctness of all ALU R-type and I-type instructions. Demonstrate the correctness of LW and SW instructions. Similarly, you should demonstrate the correctness of all branch and jump instructions.
2. Write a simple program that counts the number of 1's in a 32-bit register.
3. Write short programs and loops to verify the correctness of a sequence of instructions. Make sure that your pipelined CPU can handle data hazards and control hazards properly.
4. Write a sort procedure (selection sort, bubble sort, etc.). Write a main function to call the sort procedure and sort an array of integers in the data memory.

Document all your test programs and files and include them in the report document.

Project Report

The report document must contain sections highlighting the following:

1 – Design and Implementation

- Highlight the design choices you made and why, and any notable features that your processor has.
- Provide drawings of the various components and the overall datapath.
- Provide a complete description of the control logic and the control signals. Provide a table giving the control signal values for each instruction.
- Provide a complete description of the forwarding logic, the cases that were handled, and the logic you have implemented to handle the control hazards.

2 – Simulation and Testing

- Describe the test programs that you used to test your design with sufficient comments describing the programs, their input, and expected output. List all the instructions that were tested and work correctly. List all the instructions that do not run properly.
- Describe all the cases that you handled involving data dependences between instructions, data forwarding, and stalling the pipeline.
- Provide snapshots showing test programs and their output results.

3 – Teamwork

- Two or at most three students can form a group. Write the names of all the group members on the project report title page.
- Group members are required to coordinate their work among themselves, so that everyone is involved in design, implementation, simulation, and testing.
- Show the work done by each group member using a chart.

Submission Guidelines

All submissions will be done through Blackboard.

Attach one zip file containing all the design circuits, the test programs source code and binary instruction files that you have used to test your design, their test data, as well as the report document.

Grading policy:

The grade will be divided according to the following components:

- Correctness: whether your implementation is working.
- Completeness and testing: whether all instructions and cases have been implemented, handled, and tested properly.
- Participation and contribution to the project. It should be noted that being in a group that implemented the project correctly does not qualify you to get full mark. Your mark will depend on your contribution in the project.
- Report organization and clarity.

Submission Deadlines:

Task	Deadline
Single-cycle CPU Design Demo	Week 13
Pipelined CPU Design Demo	Week 15
Final Report Submission	Week 15